

# Savage4 Registers

## RE046-B

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This document provides detailed descriptions of the S3 Savage4 (all types) registers. The various methods of accessing these registers are described in Section 1.

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## Change History

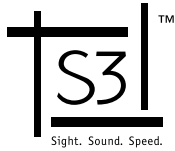
### Changes to Version A

SR1A\_1, 3: Inverts for 1x and 2x signature clock in bypass modes  
SR36, 37, 38, 39: Added duplicate DCLK PLL registers for VGA DCLK programming  
SR3D\_4: Allows HW cursor to move to right edge with flat panel and SP on (Rev. C)  
CR37\_3: Moved external 4x AGP clock input to CR37\_4  
CR37\_7: 1 (default) = 1x AGP clock from PLL; 0 = 1x AGP clock from bypass  
CR85: Revised definition for display FIFO fill/drain control.  
CR88\_4: Added restrictions on use of block write. Removed tiling off restriction.  
PCI0E\_7: Now reserved (not multifunction device)  
MM850C\_10: Reserved (MCLK only clock for 2D engine)  
MM48584\_6-4: 010 = destination (not source) color and 011 = 1-destination (not source) color  
MM81EC\_31-30: Must be programmed to 01b when destination flush enabled.

### Changes to Version 0.3

**Note: Rev. B silicon changes are in bold.**

SR1A\_0: Invert DCLK for clock doubled 15/16 bpp modes  
SR1A\_4: Now reserved = 0 (-STWR function no longer supported)  
SR35\_6: Former bit 7 is moved to bit 6. Former bit 6 is removed.  
SR35\_7: New bit reverses TV data output format selected via SR35\_5-4.  
**SR37: PANELCLK output control (Rev. B)**  
**SR39: AGP pad compensation register (Rev. B)**  
SR3D: New register for flat panel output control  
SR54\_7-5: Now reserved  
SR58: Revised definition of horizontal border  
SR5B\_7-4: Revised vertical expansion table  
SR5A: Revised definition of vertical border  
CR11\_6: Reserved (CR3A controls refresh)  
CR33\_7: Reserved (no flicker filter)  
**CR36\_7-5: Added support for 8 and 32 MB 2Mx32 SDRAM configurations (Rev. B)**  
**CR37\_3: Added external clocks enabled by this bit (Rev. B)**  
CR3A\_1-0: Revised definition for memory refresh control  
CR3F\_7-6: Reserved (no video engine or TV)  
CR4C: Corrected valid bit range.  
CR4D\_1-0: Reserved (4K alignment)  
**CR59: Changed definition because of new memory map (Rev. B)**  
CR60\_3-0: Added skew control for SDCLK1, SDCLK2 and SDCLKOUT.  
**CR68\_7-6: Added definitions for 2Mx32 4 bank and 4Mx16 4 bank SDRAM support (Rev. B)**  
CR6F\_0: Added note that this bit should be set only to allow programming of CR3F and then must be cleared  
CR70\_5: Added bit to eliminate an AGP clock delay  
CR87\_0: 1 or 2 clock block write  
CR87\_5-4: Specify clock rate for refresh  
CR90\_3 and CR90\_6: These two bits must be set when displaying a 15/16 or 32 bpp primary stream on a flat panel.  
**CR92\_4: Read only bit, 0 = Savage4 LT (Rev. B)**  
CR92\_6: New bit for 2Mx32 4 bank SDRAM support



**CRB6: Write only register new pad compensation code (Rev. B)**

**CRB7: AGP 2x clock skew control (Rev. B)**

**PCI10-PCI24: New base address definitions (Rev. B)**

MM8218\_19-16: Value is in units of tiles (not QWords)

MM8218\_23-20: Value is in units of lines (not QWords)

MM8508\_4, 12: Removed (no BFIFO)

MMFF00\_18, 19, 31: Reserved (no video conferencing support)

MMFF08\_5, 6: Reserved (no video conferencing support)

MMFF1C: Removed (LPB general I/O port not supported)

**MM81C0\_31-28: Added bits to support triple buffering (Rev. B)**

**MM8218\_31-24: Added new tile boundary field with QWord units (Rev. B)**

**MM48508, MM48528, MM48548: New Vertex Z coordinate registers (Rev. B)**

**MMr8580: Removed Z Pixel Offset register (Rev. B)**

MM48584\_30: Noted that the destination write low watermark must be all 0's if this bit is set.

MM48584\_31: Noted that the Z write low watermark must be all 0's if this bit is set.

MM485A4\_15-0: Modified definition for texture transparent color for RGB modes.

**MM485A8\_27: Reserved (no disable for perspective correction (Rev. B)**

**MM485D4\_31: Changed to select W or Z buffer (Rev. B)**

MM485E8\_21-16: Noted this value must be all 0's if MM48584\_31 is set to 1 (flushing enabled). **Further revised for Rev. B.**

MM485EC\_17-12: Noted this value must be all 0's if MM48584\_30 is set to 1 (flushing enabled). **Further revised for Rev. B.**

**MM48C00: New definition of Status Word 0 for Rev. B**

MM48C10: Definitions of stop and resume writing thresholds are reversed. **For Rev. B, values are in 32 DWord units instead of DWords.**

**MM48C60: New definition of Alternate Status Word 0 for Rev. B**

### Changes to Version 0.2

SR39\_7-6: Added bits for output drive adjustment for 1.5V VDDq

MM8300\_210: Primary Stream buffer size in QWords -1

MM8304\_21-0: Secondary Stream buffer size in QWords - 1

MM48A00\_20-3: Corrected requirement for bits 5-3 (must be 111).

MM48A00\_26-25: Noted restrictions on oversampling.

MM485EC\_5-0: Reserved (no low watermark)

MM485EC\_11-6: Revised definition of high watermark

# Table of Contents

<b>Change History</b> .....	<b>ii</b>
Changes to Version 0.3 .....	ii
MM48C60: New definition of Alternate Status Word 0 for Rev. B .....	iii
<b>Table of Contents</b> .....	<b>iv</b>
<b>Section 1. Register Addressing</b> .....	<b>1</b>
1.1 PROGRAMMED I/O .....	1
1.2 MMIO .....	1
1.3 BURST COMMAND INTERFACE (BCI).....	4
<b>Section 2: VGA Register Descriptions</b> .....	<b>5</b>
2.1 GENERAL REGISTERS.....	5
2.2 SEQUENCER REGISTERS.....	8
2.3 CRT CONTROLLER REGISTERS.....	12
2.4 GRAPHICS CONTROLLER REGISTERS .....	25
2.5 ATTRIBUTE CONTROLLER REGISTERS .....	31
2.6 RAMDAC REGISTERS .....	36
<b>Section 3: Extended Sequencer Register Descriptions</b> .....	<b>39</b>
<b>Section 4: Flat Panel Registers</b> .....	<b>55</b>
<b>Section 5: Extended CRTC Register Descriptions</b> .....	<b>69</b>
<b>Section 6: PCI Register Descriptions</b> .....	<b>113</b>
<b>Section 7: 2D Graphics Engine Register Descriptions</b> .....	<b>129</b>
<b>Section 8: Streams Processor Register Descriptions</b> .....	<b>151</b>
<b>Section 9: LPB/VIP Register Descriptions</b> .....	<b>171</b>
<b>Section 10: 3D Engine Register Descriptions</b> .....	<b>187</b>
<b>Section 11: Motion Compensation Register Descriptions</b> .....	<b>209</b>
<b>Section 12: Mastered Data Transfer Register Descriptions</b> .....	<b>217</b>
<b>Section 13: Configuration/Status Register Descriptions</b> .....	<b>223</b>
<b>Index</b> .....	<b>233</b>

## Section 1. Register Addressing

There are three methods of programming Savage4 registers:

- Programmed I/O
- MMIO
- Burst Command Interface (BCI)

In addition, the CPU can directly access video memory via several data transfer windows (linear and tiled addressing) and write image data to video memory via the 2D or 3D engine via another data transfer window. Each of these topics is discussed below.

Note: Software should write 0s to all reserved register bits.

### 1.1 PROGRAMMED I/O

Programmed I/O (i.e., use of the processor's IN and OUT instructions), can be used only for accessing registers in the standard VGA register space. These include all the registers described in Sections 2 through 5. Sections 3-5 describe registers defined by S3 that use extensions of the VGA sequencer and CRTC register indices. These registers are denoted by "SRxx" and "CRxx", with xx being the index.

All the standard VGA register and extensions are also accessible via memory mapped I/O (MMIO), except that 3C3H must always be accessed via I/O. Setting SR9\_7 to 1 disables all I/O accesses except to the standard VGA address space. PCI02\_0 = 0 disables all I/O accesses.

### 1.2 MMIO

MMIO enabled is the power-on default, allowing PCI software immediate access to all registers and the ability to relocate the address space. There are two MMIO address mappings, as determined by the state of CRB0\_7. By default, CRB0\_7 = 1, which selects Mapping 0. The definitions of Mapping 0 and Mapping 1 change from Rev. A silicon to Rev. B silicon, as explained below. For processors that support it, the address ranges with bases specified by PCI14, 18, 1C, 20 and 24 should be marked as write combining. The address range with the base specified by PCI10 should not.

Register Addressing

**PCI Base Address 0 (PCI10) - Mapping 0 and Mapping 1**

For Rev. A silicon, bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. For Rev. B silicon, bits 31-19 are programmable, resulting in a 512-KByte address space being claimed. The default base address is 7000 0000H. Write combining cannot be used for this address range.

Offset from Base	Size	Description	Access with BCI Active
0x0000 0000 – 0x0000 7FFF	32K	Image Data Transfer Area	
0x0000 8000 – 0x0000 807F	64	PCI Configuration Registers	No
0x0000 8080 – 0x0000 80FF	64	AGP Configuration Registers	No
0x0000 8100 – 0x0000 817F	128	Packed 2D Enhanced Registers	No
0x0000 8180 – 0x0000 82E4	164	Streams Processor Registers	Yes
0x0000 82E8	4	Current Y Position Register (2D engine)	No
0x0000 8300 – 0x0000 83AF	176	Streams Processor extensions	Yes
0x0000 83B0 – 0x0000 83BF	16	VGA 3B? Registers	No
0x0000 83C0 – 0x0000 83CF	16	VGA 3C? Registers	No
0x0000 83D0 – 0x0000 83DF	16	VGA 3D? Registers	No
0x0000 83E0 - 0x0000 8500	288	Unused	No
0x0000 8504 – 0x0000 8510	16	System Registers	Yes (except 8504)
0x0000 8514 - 0x0000 86E4	468	Unused	No
0x0000 86E8 - 0x0000 F6FF	28K	Non-packed 2D registers	No
0x0000 F700 - 0x0000 FEFF	2K	Unused	No
0x0000 FF00 - 0x0000 FFFF	256	LPB/VIP Registers	Yes
0x0001 0000 - 0x0002 FFFF	128K	Burst Command Data	
0x0003 0000 - 0x0004 84FF	97K	Unused	
0x0004 8500 - 0x0004 88FF	1024	3D Registers	No
0x0004 8900 - 0x0004 89FF	256	Motion Compensation Registers	No (Note 1)
0x0004 8A00 - 0x0004 8AFF	512	MEU Registers	No (Note 1)
0x0004 8C00 - 0x0004 8CFF	256	Configuration and Status Registers	Yes (except 8C20-8C24)
0x0004 8D00 - 0x00FF FFFF	15.7M	Unused (not available in Rev. B)	

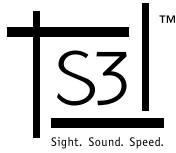
When registers are being directly accessed via MMIO (not using the BCI), the BCI function should be idle for access to the registers indicated by "No" in the right column of the above table.

Note 1: MMIO writes to motion compensation registers must only be done with BCI disabled. Reads can be done with BCI enabled.

**PCI Base Address 1 (PCI14) - Mapping 0) (Rev. A or Rev B)**

Bits 31-27 of the base address are programmable, resulting in a 128-MByte address space being claimed. The default base address is 6000 0008H (prefetching allowed).

Offset from Base	Size	Description
0x0000 0000 – 0x01FF FFFF	32M	Linear Frame Buffer Access Area
0x0200 0000 – 0x02FF FFFF	16M	Tiled Addressing Aperture 0
0x0300 0000 – 0x03FF FFFF	16M	Tiled Addressing Aperture 1
0x0400 0000 – 0x04FF FFFF	16M	Tiled Addressing Aperture 2
0x0500 0000 – 0x05FF FFFF	16M	Tiled Addressing Aperture 3
0x0600 0000 – 0x06FF FFFF	16M	Tiled Addressing Aperture 4
0x0700 0000 – 0x0701 FFFF	128K	Burst Command Data

**Rev A Mapping 1****PCI Base Address 1 (PCI14) - Mapping 1) (Rev A)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6000 0008H (prefetching allowed).

Offset from Base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	First 16M Linear Frame Buffer Access Area

**PCI Base Address 2 (PCI18) - Mapping 1) (Rev. A)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6800 0008H (prefetching allowed).

Offset from Base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	Second 16M Linear Frame Buffer Access Area

**PCI Base Address 3 (PCI1C) - Mapping 1) (Rev. A)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6200 0008H (prefetching allowed).

Offset from Base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	Tiled Addressing Aperture 0

**PCI Base Address 4 (PCI20) - Mapping 1) (Rev A)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6300 0008H (prefetching allowed).

Offset from Base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	Tiled Addressing Aperture 1

**PCI Base Address 5 (PCI24) - Mapping 1) (Rev. A)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6400 0008H (prefetching allowed).

Offset from the base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	Tiled Addressing Aperture 2

**Rev. B Mapping 1****PCI Base Address 1 (PCI14) - Mapping 1) (Rev B)**

Bits 31-25 of the base address are programmable, resulting in a 32-MByte address space being claimed. The default base address is 6000 0008H (prefetching allowed).

Offset from Base	Size	Description
0x0000 0000 – 0x02FF FFFF	32M	32M Linear Frame Buffer Access Area

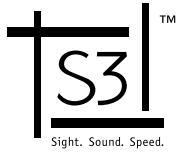
**PCI Base Address 2 (PCI18) - Mapping 1) (Rev. B)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6800 0008H (prefetching allowed).

Offset from Base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	Tiled Addressing Aperture 0

**PCI Base Address 3 (PCI1C) - Mapping 1) (Rev. B)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6200 0008H (prefetching allowed).



Offset from Base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	Tiled Addressing Aperture 1

**PCI Base Address 4 (PCI20) - Mapping 1) (Rev B)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6300 0008H (prefetching allowed).

Offset from Base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	Tiled Addressing Aperture 2

**PCI Base Address 5 (PCI24) - Mapping 1) (Rev. B)**

Bits 31-24 of the base address are programmable, resulting in a 16-MByte address space being claimed. The default base address is 6400 0008H (prefetching allowed).

Offset from the base	Size	Description
0x0000 0000 – 0x01FF FFFF	16M	Tiled Addressing Aperture 3

### 1.3 BURST COMMAND INTERFACE (BCI)

This interface allows bursts of commands (register writes) and data to be transferred from the CPU, PCI bus and/or system memory to the Savage4 registers and the frame buffer. The BCI is the most efficient method of generating most of the display effects possible with Savage4. Its use minimizes CPU and memory bandwidth usage, minimizes system bus traffic and provides automatic coordination/synchronization among competing tasks.

The BCI interface is enabled by MM48C18\_3 = 1. A series of 32-bit writes containing instructions and data is then burst to Savage4 using any address in the 128K range from 101 000H to 102 FFFFH. Each 32-bit write fills one slot of a 32-slot FIFO (if there is space), from which the data is automatically read out, interpreted and executed. If the on-chip queue fills up, additional BCI writes can be stored in an overflow circular buffer located in the frame buffer at an address specified by MM48C14\_13-0. Its size is specified by MM48C14\_31-29.

Software needs to monitor the queue status to determine if there is a shortage or excess of command data. A read of MM48C00\_16-0 provides the number of filled entries in the command queue (both on- and off-chip). To minimize CPU and system bus usage, Savage4 optionally provides this information via a read of cacheable system memory. This is called shadow status, and is enabled by setting MM48C0C\_0 and MM48C18\_1 to 1. The address of the start of the status information in system memory is programmed in MM48C0C\_31\_5. This status information consists of the data from Status Word registers 0-2. It is automatically written to system memory when the command buffer (on- and off-chip) is almost full (as specified by a watermark programmed in MM48C10\_31-16 and when the command buffer is almost empty (as specified by a watermark programmed in MM48C10\_15-0). The update can also be forced by an UpdateShadowStatus BCI command issued by software. As a result of this update policy, the shadow status will normally be accurate for a only a short time. Exact status is always available by direct reading of the Status Word registers.



## Section 2: VGA Register Descriptions

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). A question mark in an address stands for a hexadecimal value of either 'B' or 'D'. If bit 0 of the Miscellaneous Output Register (3C2H, Write) is set to 1, the address is based at 3DxH for color emulation. If this bit is reset to 0, the address is based at 3BxH for monochrome emulation.

### 2.1 GENERAL REGISTERS

This section describes general input status and output control registers.

---

#### Miscellaneous Output Register

Write Only                      Address: 3C2H

Read Only                        Address: 3CCH

Power-On Default: 00H

This register controls miscellaneous output signals. A hardware reset sets all bits to zero.

7	6	5	4	3	2	1	0
VSP	HSP	PGS	= 0	CLK	SEL	ENB	IOA
				1	0	RAM	SEL

Bit 0            IOA SEL - I/O Address Select  
0 = Monochrome emulation. Address based at 3Bx  
1 = Color emulation. Address based at 3Dx

Bit 1            ENB RAM - Enable CPU Display Memory Access  
0 = Disable access of the display memory from the CPU  
1 = Enable access of the display memory from the CPU

Bits 3-2        Clock Select - Select the Video Clock Frequency  
00 = Selects 25.175 MHz DCLK for 640 horizontal pixels  
01 = Selects 28.322 MHz DCLK for 720 horizontal pixels  
10 = Reserved  
11 = Enables loading of DCLK PLL parameters in SR12 and SR13.

A setting of either 00b or 01b causes the appropriate values to be programmed into the DCLK PLL registers if bit 1 of SR15 is set to 1.

Bit 4            Reserved = 0

Bit 5            PGS -Select High 64K Page  
0 = Select the low 64K page of memory  
1 = Select the high 64K page of memory

Bit 6            HSP - Select Negative Horizontal Sync Pulse  
0 = Select a positive horizontal retrace sync pulse  
1 = Select a negative horizontal retrace sync pulse

Bit 7            VSP - Select Negative Vertical Sync Pulse  
0 = Select a positive vertical retrace sync pulse  
1 = Select a negative vertical retrace sync pulse

**Feature Control Register**

Write Only                      Address: 3?AH

Read Only                      Address: 3CAH

Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	VSSL	= 0	= 0	= 0

Bits 2-0              Reserved = 0

Bit 3                  VSSL - Vertical Sync Type Select

0 = Enable normal vertical sync output to the monitor

1 = The `vertical sync' output is the logical OR of `vertical sync' and `vertical active display enable' (an internal signal)

Bits 7-4              Reserved = 0

**Input Status 0 Register**

Read Only                      Address: 3C2H

Power-On Default: Undefined

This register indicates the status of the VGA adapter.

7	6	5	4	3	2	1	0
CRT INTPE	= 0	= 0	MON SEN	= 0	= 0	= 0	= 0

Bits 3-0              Reserved = 0

Bit 4                  MON SEN - Monitor Sense Status

0 = The internal SENSE signal is a logical 0

1 = The internal SENSE signal is a logical 1

Bits 6-5              Reserved = 0

Bit 7                  CRT INTPE - CRT Interrupt Status

0 = Vertical retrace interrupt cleared

1 = Vertical retrace interrupt pending

**Input Status 1 Register**

Read Only                      Address: 3?AH

Power-On Default: Undefined

This register indicates video sync timing and video wraparound.

7	6	5	4	3	2	1	0
= 0	= 0	TST-VDT		VSY	= 1	R	DTM
		1 0					

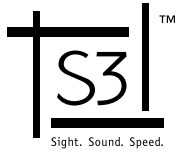
Bit 0                  DTM - Display Mode Inactive

0 = The display is in the display mode.

1 = The display is not in the display mode. Either the horizontal or vertical retrace period is active

Bit 1                  Reserved = 0

Bit 2                  Reserved = 1



Bit 3 VSY - Vertical Sync Active  
0 = Display is in the display mode  
1 = Display is in the vertical retrace mode

Bits 5-4 TST-VDT - Video Signal Test  
  
Video Data Feedback 1,0. These bits are feedback video signals to do read back tests. These bits are selectively connected to two of the eight color outputs of the attribute controller. Bits 5 and 4 of the color plane enable register (AR12) control the multiplexer for this video output observation.

Bits 7-6 Reserved = 0

**Video Subsystem Enable Register**

Write Only Address: 3C3H  
Power-On Default: 00H

This register is only accessible via its I/O address (not MMIO). For enabling via MMIO, use MM8510\_0.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	CF ENB

Bit 0 CF ENB - Chip Function Enable  
0 = Chip function disabled  
1 = Chip function enabled

Bits 7-1 Reserved

## 2.2 SEQUENCER REGISTERS

The sequencer registers (including the S3 extensions) are located at two address spaces. These registers are accessed by first writing sequencer register index at address 3C4H and then writing to or reading from the data register at 3C5H. A word write of both address and data at 3C4H can also be performed.

---

### Sequencer Index Register

Read/Write Address: 3C4H  
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	SEQUENCER REGISTER INDEX					

Bits 4-0 SEQUENCER REGISTER INDEX

Value = Index of the sequencer register where data is to be accessed

Bits 7-5 Reserved

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### Sequencer Data Register

Read/Write Address: 3C5H  
Power-On Default: Undefined

7	6	5	4	3	2	1	0
SEQUENCER REGISTER DATA							

Bits 7-0 SEQUENCER REGISTER DATA

Value = Data read from or to be written to the sequencer register at the index programmed in 3C4H.

---

### Reset Register (SR0)

Read/Write Address: 3C5H, Index 00H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	SYN RST	ASY RST

Bit 0 ASY RST - Asynchronous Reset  
This bit is for VGA software compatibility only. It has no function for Savage4

Bit 1 SYN RST - Synchronous Reset  
This bit is for VGA software compatibility only. It has no function for Savage4.

Bits 7-2 Reserved = 0

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**Clocking Mode Register (SR1)**

Read/Write                      Address: 3C5H, Index 01H

Power-On Default: 00H

This register controls the operation mode of dot clock and character clock.

7	6	5	4	3	2	1	0
= 0	= 0	SCR OFF	SHF 4	CCK 1/2	SHF LD	= 0	8DC

- Bit 0            8DC - 8 Dot Clock Select  
 0 = Character clocks 9 dots wide are generated  
 1 = Character clocks 8 dots wide are generated
- Bit 1            Reserved = 0
- Bit 2            SHF LD - Load Serializers Every Second Character Clock  
 0 = Load the video serializer every character clock  
 1 = Load the video serializers every other character clock
- Bit 3            CCK 1/2 - Internal Character Clock/2  
 0 = Internal character clock is unchanged  
 1 = Halve the frequency of the internal character clock
- This bit is used for horizontal pixel doubling.
- Bit 4            SHF 4 - Load Serializers Every Fourth Character Clock  
 0 = Load the serializers every character clock cycle  
 1 = Load the serializers every fourth character clock cycle
- Bit 5            SCR OFF - Screen Off  
 0 = Screen is turned on.  
 1 = Screen is turned off
- Bits 7-6        Reserved = 0

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**Enable Write Plane Register (SR2)**

Read/Write                      Address: 3C5H, Index 02H

Power-On Default: 00H

This register selects write protection or write permission for CPU write access into video memory.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	EN.WT.PL.			

- Bits 3-0        EN.WT.PL - Enable Write to a Plane  
 0 = Disables writing into the corresponding plane  
 1 = Enables the CPU to write to the corresponding color plane
- Bits 7-4        Reserved = 0

**Character Font Select Register (SR3)**

Read/Write Address: 3C5H, Index 03H  
Power-On Default: 00H

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
= 0	= 0	SLA 2	SLB 2	SLA 1 0		SLB 1 0	

In text modes, bit 3 of the attribute byte normally turns the foreground intensity on or off. This bit can be redefined to be a switch between two character sets. The switch is enabled when there is a difference between the value of character font select A and character font select B bits. Memory Mode (SR4) register bit 1 = 1 (extended memory) enables all bits of this function; otherwise character fonts 0 and 4 are available. 256 KBytes of video memory support 8 character sets. This register is reset to 0 asynchronously during a system reset.

Bits 4, 1-0 SLB - Select Font B

Value = the portion of plane 2 used to generate text character fonts when bit 3 of the attribute byte is a logical 1, according to the following table:

<b>Bits 4,1,0</b>	<b>Font Table Location</b>	<b>Bits 4, 1,0</b>	<b>Font Table Location</b>
000	First 8K of plane 2	100	Second 8K of plane 2
001	Third 8K of plane 2	101	Fourth 8K of plane 2
010	Fifth 8K of plane 2	110	Sixth 8K of plane 2
011	Seventh 8K of plane 2	111	Eighth 8K of plane 2

Bits 5, 3-2 SLA - Select Font A

Value = the portion of plane 2 used to generate text character fonts when bit 3 of attribute byte is a logical 0, according to the same table as the character font select A.

Bits 7-6 Reserved = 0

---

**Memory Mode Control Register (SR4)**

Read/Write Address: 3C5H, Index 04H  
Power-On Default: 00H

This register controls CPU memory addressing mode.

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
= 0	= 0	= 0	= 0	CHN 4M	SEQ MOD	EXT MEM	= 0

Bit 0 Reserved = 0

Bit 1 EXT MEM - Extended Memory Access  
0 = Memory access restricted to 16/32 KBytes  
1 = Allows complete memory access to 256 KBytes. Required for VGA

Bit 2 SEQ MOD - Sequential Addressing Mode  
0 = Enables the odd/even addressing mode. Even addresses access planes 0 and 2. Odd addresses access planes 1 and 3  
1 = Directs the system to use a sequential addressing mode

This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.

Bit 3 CHN 4M - Select Chain 4 Mode  
0 = Enables odd/even mode  
1 = Chain 4 mode

This bit selects modulo 4 addressing for CPU access to display memory. A logical 1 directs the two lower order bits of the CPU address used to select the plane in video memory to be accessed as follows:

A1	A0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bits 7-4 Reserved = 0

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## 2.3 CRT CONTROLLER REGISTERS

The CRT controller registers (including S3 extensions) are located at two addresses. These registers are accessed by first writing to the index register of the CRT controller and then accessing the data register. The index register is located at address 3?4H and the data register is at 3?5H. Which address is used (3BX or 3DX) depends on bit 0 of the Miscellaneous Output register at 3C2H. A word write of both address and data at 3?4H can also be performed.

---

### CRT Controller Index Register

Read/Write Address: 3?4H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
CRTC REGISTER INDEX							

Bits 7-0 CRTC REGISTER INDEX

Value = Index of the CRTC register to be accessed

---

### CRT Controller Data Register

Read/Write Address: 3?5H  
Power-On Default: Undefined

This register is the data port for the CRT controller register indexed by the CRT Controller Address register.

7	6	5	4	3	2	1	0
CRTC REGISTER DATA							

Bits 7-0 CRTC REGISTER DATA

Value = Data read from or to be written to the CRTC controller register at the index specified in 3?4H.

---

### Horizontal Total Register (CR0)

Read/Write Address: 3?5H, Index 00H  
Power-On Default: Undefined

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active. In other words, it is the total time required for both the displayed and non-displayed portions of a single scan line. The value in this register may affect the value required in CR3B.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL 7-0							

Bits 7-0 HORIZONTAL TOTAL 7-0

11-bit Value = (number of character clocks in one scan line) - 5.

Bit 8 of this value is bit 0 of CR5D. Bits 10-9 are CR5F\_1-0.



---

**Horizontal Display End Register (CR1)**

Read/Write                      Address: 3?5H, Index 01H

Power-On Default: Undefined

This register defines the number of character clocks for one line of the active display.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY END 7-0							

Bits 7-0            HORIZONTAL DISPLAY END 7-0

11-bit Value = (number of character clocks of active display) - 1.

Bit 8 of this value is bit 1 of CR5D. Bits 10-9 are CR5F\_3-2.

---

**Start Horizontal Blank Register (CR2)**

Read/Write                      Address: 3?5H, Index 02H

Power-On Default: Undefined

This register specifies the value of the character clock counter at which the BLANK signal is asserted.

7	6	5	4	3	2	1	0
START HORIZONTAL BLANK 7-0							

Bits 7-0            START HORIZONTAL BLANK 7-0

11-bit Value = character clock value at which horizontal blanking begins.

Bit 8 of this value is bit 2 of CR5D. Bits 10-9 are CR5F\_5-4.

---

**End Horizontal Blank Register (CR3)**

Read/Write                      Address: 3?5H, Index 03H

Power-On Default: Undefined

This register determines the pulse width of the BLANK signal and the display enable skew.

7	6	5	4	3	2	1	0
R	DSP-SKW 1 0		END HORIZONTAL BLANK 4-0				

Bits 4-0            END HORIZONTAL BLANK 4-0

6-bit Value = least significant 6 bits of the character clock counter value at which time horizontal blanking ends

To obtain this value, add the desired BLANK pulse width in character clocks to the Start Horizontal Blank value, which is also in character clocks. Bit 5 of this value is CR5\_7. If the horizontal blank period is more than 64 character clocks, CR5D\_3 must be set to 1.

If CR5D\_7 is set to 1 for 1280x1024x24 mode, CR5B\_5-4 become bits 7-6 of this value and CR5D\_3 is set to 1 when the blank period is greater than 256 character clocks.

Bits 6-5      DSP-SKW - Display Skew  
 00 = Zero character clock skew  
 01 = One character clock skew  
 10 = Two character clock skew  
 11 = Three character clock skew

These two bits determine the amount of display enable skew. Display enable skew control provides sufficient time for the CRT Controller to access the display buffer to obtain a character and attribute code, access the character generator font, and then go through the Horizontal Pixel Panning register in the Attribute Controller. Each access requires the display enable signal to be skewed one character clock unit so the video output is synchronous with the HSYNC and VSYNC signals. The bit values and amount of skew are shown in the following table:

Bit 7          Reserved

---

**Start Horizontal Sync Position Register (CR4)**

Read/Write                      Address: 3?5H, Index 04H  
 Power-On Default: Undefined

This register is used to adjust the screen center horizontally and to specify the character position at which HSYNC becomes active.

7	6	5	4	3	2	1	0
START HORIZONTAL SYNC POSITION 7-0							

Bits 7-0          START HORIZONTAL SYNC POSITION 7-0  
 11-bit Value = character clock counter value at which HSYNC becomes active.  
 Bit 8 of this value is bit 4 of CR5D. Bits 10-9 are SR5F\_7-6.

---

**End Horizontal Sync Position Register (CR5)**

Read/Write                      Address: 3?5H, Index 05H  
 Power-On Default: Undefined

This register specifies when the HSYNC signal becomes inactive and the horizontal skew.

7	6	5	4	3	2	1	0
EHB B5	HOR-SKW 1 0	END HORIZONTAL SYNC POS 4-0					

Bits 4-0          END HORIZONTAL SYNC POS 4-0  
 5-bit Value = 5 least significant bits of the character clock counter value at which time HSYNC becomes inactive.  
 To obtain this value, add the desired HSYNC pulse width in character clocks to the Start Horizontal Sync Position value, also in character clocks. If the horizontal sync period is more than 32 character clocks, bit 5 of CR5D must be set to 1.  
 If CR5D\_7 is set to 1 for 1280x1024x24 mode, CR5B\_7-6 become bits 6-5 of this value and CR5D\_5 is set to 1 when the sync period is greater than 128 character clocks.

Bits 6-5      HOR-SKW - Horizontal Skew  
 00 = Zero character clock skew  
 01 = One character clock skew  
 10 = Two character clock skew  
 11 = Three character clock skew

These bits control the skew of the HSYNC signal. A binary 00 equals no HSYNC delay. For some modes, it is necessary to provide an HSYNC signal that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the HSYNC signal. To guarantee the signals are latched properly, HSYNC is asserted before the end of the display enable signal, and then skewed several character clock times to provide the proper screen centering.

Bit 7      EHB B5 - End Horizontal Blanking Bit 5

---

**Vertical Total Register (CR6)**

Read/Write                      Address: 3?5H, Index 06H  
 Power-On Default: Undefined

This register specifies the number of scan lines from one VSYNC active to the next VSYNC active. The scan line counter resets to 0 at this point.

7	6	5	4	3	2	1	0
VERTICAL TOTAL 7-0							

Bits 7-0      VERTICAL TOTAL 7-0

11-bit Value = (number of scan lines from VSYNC active to the next VSYNC active) - 2

Bit 8 is CR7\_0. Bit 9 is CR7\_5. Bit 10 is CR5E\_0.

---

**CRTC Overflow Register (CR7)**

Read/Write                      Address: 3?5H, Index 07H  
 Power-On Default: Undefined

7	6	5	4	3	2	1	0
VRS	VDE	VT	LCM	SVB	VRS	VDE	VT
9	9	9	8	8	8	8	8

- Bit 0      Bit 8 of the Vertical Total register (CR6)
- Bit 1      Bit 8 of the Vertical Display End register (CR12)
- Bit 2      Bit 8 of the Vertical Retrace Start register (CR10)
- Bit 3      Bit 8 of the Start Vertical Blank register (CR15)
- Bit 4      Bit 8 of the Line Compare register (CR18)
- Bit 5      Bit 9 of the Vertical Total register (CR6)
- Bit 6      Bit 9 of the Vertical Display End register (CR12)
- Bit 7      Bit 9 of the Vertical Retrace Start register (CR10)

**Preset Row Scan Register (CR8)**

Read/Write Address: 3?5H, Index 08H

Power-On Default: Undefined

This register is used for the pixel scrolling and panning, and text formatting and vertical scrolling.

7	6	5	4	3	2	1	0
= 0	BYTE-PAN 1 0		PRE-SET ROW SCAN COUNT				

Bits 4-0 PRE-SET ROW SCAN COUNT

Value = starting row within a character cell for the first character row displayed after vertical retrace

This allows a partial character row to be displayed at the top of the display and is used for scrolling.

Bits 6-5 BYTE-PAN

Value = number of bytes to pan

The number of pixels to pan is specified in AR13.

Bit 7 Reserved = 0

**Maximum Scan Line Register (CR9)**

Read/Write Address: 3?5H, Index 09H

Power-On Default: Undefined

This register specifies the number of scan lines per character row and provides one scanning control bit and two overflow bits.

7	6	5	4	3	2	1	0
DBL SCN	LCM 9	SVB 9	MAX SCAN LINE				

Bits 4-0 MAX SCAN LINE

Value = (number of scan lines per character row) - 1

Bit 5 SVB 9 - Bit 9 of the Start Vertical Blank Register (CR15)

Bit 6 LCM 9 - Bit 9 of the Line Compare Register (CR18)

Bit 7 DBL SCN

0 = Normal operation

1 = Enables double scanning operation

When this bit is set, each line is displayed twice by repeating the row scan counter and video memory address.

Vertical parameters in the CRT controller are not affected.

**Cursor Start Scan Line Register (CRA)**

Read/Write Address: 3?5H, Index 0AH

Power-On Default: Undefined

The cursor start register defines the row scan of a character line where the cursor begins.

7	6	5	4	3	2	1	0
= 0	= 0	CSR OFF	CSR CURSOR START SCAN LINE				

Bits 4-0 CSR CURSOR START SCAN LINE

Value = (starting cursor row within the character cell) - 1

When the cursor start register is programmed with a value greater than the cursor end register, no cursor is generated.

Bit 5 CSR OFF

 0 = Turns on the text cursor  
 1 = Turns off the text cursor

Bits 7-6 Reserved = 0

**Cursor End Scan Line Register (CRB)**

Read/Write Address: 3?5H, Index 0BH

Power-On Default: Undefined

This register defines the row scan of a character line where the cursor ends.

7	6	5	4	3	2	1	0
= 0	CSR-SKW 1 0		CURSOR END SCAN LINE				

Bits 4-0 CURSOR END SCAN LINE

Value = ending scan line number within the character cell for the text cursor

If the value of the cursor start line is greater than the value of cursor end line, then no cursor is generated.

Bits 6-5 CSR-SKW - Cursor Skew

 00 = Zero character clock skew  
 01 = One character clock skew  
 10 = Two character clock skew  
 11 = Three character clock skew

These bits control the delay skew of the cursor signal. Cursor skew delays the text cursor by the selected number of clocks. For example, a skew of 1 moves the cursor right one character position on the screen.

Bit 7 Reserved = 0

---

**Start Address High Register (CRC)**

Read/Write                      Address: 3?5H, Index 0CH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS (HIGH)							

Bits 7-0            DISPLAY START ADDRESS (HIGH)

23-bit Value = the first address after a vertical retrace at which the display on the screen begins on each screen refresh

These along with bits 6-0 of CR69 are the high order start address bits.

---

**Start Address Low Register (CRD)**

Read/Write                      Address: 3?5H, Index 0DH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS (LOW)							

Bits 7-0            DISPLAY START ADDRESS (LOW)

Value = the 8 low order bits of the start address

---

**Cursor Location Address High Register (CRE)**

Read/Write                      Address: 3?5H, Index 0EH

Power-On Default: Undefined

15	14	13	12	11	10	9	8
CURSOR LOCATION ADDRESS (HIGH)							

Bits 7-0            CURSOR LOCATION ADDRESS (HIGH)

23-bit Value = the cursor location address of the video memory where the text cursor is active

This register along with bits 6-0 of CR69 are the high order bits of the address.

**Cursor Location Address Low Register (CRF)**

Read/Write Address: 3?5H, Index 0FH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
CURSOR LOCATION ADDRESS (LOW)							

Bits 7-0 CURSOR LOCATION ADDRESS (LOW)

Value = the 8 low order bits of the cursor location address.

**Vertical Retrace Start Register (CR10)**

Read/Write Address: 3?5H, Index 10H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
VERTICAL RETRACE START 7-0							

Bits 7-0 VERTICAL RETRACE START 7-0

11-bit Value = scan line counter value at which VSYNC becomes active

Bit 8 is CR7\_2. Bit 9 is CR7\_7. Bit 10 is CR5E\_4.

**Vertical Retrace End Register (CR11)**

Read/Write Address: 3?5H, Index 11H

Power-On Default: 00H

This register controls the vertical interrupt and CR0-7

7	6	5	4	3	2	1	0
LOCK R0-7	REF 3/5	DIS VINT	CLR VINT	VERTICAL RETRACE END			

Bits 3-0 VERTICAL RETRACE END

Value = least significant 4 bits of the scan line counter value at which VSYNC goes inactive

To obtain this value, add the desired VSYNC pulse width in scan line units to the CR10 value, also in scan line units. The 4 least significant bits of this sum are programmed into this field. This allows a maximum VSYNC pulse width of 15 scan line units.

Bit 4 CLR VINT - Clear Vertical Retrace Interrupt

0 = Vertical retrace interrupt cleared

1 = The flip-flop is able to catch the next interrupt request

At the end of active vertical display time, a flip-flop is set for a vertical interrupt. The output of this flip-flop goes to the system interrupt controller. The CPU has to reset this flip-flop by writing a logical 0 to this bit while in the interrupt process, then set the bit to 1 to allow the flip-flop to catch the next interrupt request. Do not change the other bits in this register. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Bit 5 DIS VINT - Disable Vertical Interrupt

0 = Vertical retrace interrupt enabled if CR32\_4 = 1

1 = Vertical interrupt disabled. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on

- Bit 6      Reserved
- Bit 7      LOCK R0-7 - Lock Writes to CRT Controller Registers  
 0 = Writing to all CRT Controller registers enabled  
 1 = Writing to all bits of CR0-CR7 except CR7\_4 disabled

This bit is set to 1 by the BIOS during a mode set, a reset or power-on

---

**Vertical Display End Register (CR12)**

Read/Write                      Address: 3?5H, Index 12H  
 Power-On Default: Undefined

The vertical display enable end register defines 8 bits of the 10-bit address of the scan line where the display on the screen ends.

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END 7-0							

Bit 7-0      VERTICAL DISPLAY END 7-0

11-bit Value = (number of scan lines of active display) - 1

Bit 8 and Bit 9 are bits 1 and 6 of CR7. Bit 10 is CR5E\_1.

---

**Offset Register (CR13)**

Read/Write                      Address: 3?5H, Index 13H  
 Power-On Default: Undefined

This register specifies the logical line width of the screen and is sometimes called the screen pitch. The starting memory address for the next display row is larger than the current row by two, four or eight times this amount. If these bits are 00b, bit 2 of CR43 is extension bit 8 of this register.

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH 7-0							

Bits 7-0      LOGICAL SCREEN WIDTH 7-0

10-bit Value = quantity that is multiplied by 2 (word mode), 4 (doubleword mode) or 8 (quadword mode) to specify the difference between the starting byte addresses of two consecutive scan lines.

The addressing mode is specified by bit 6 of CR14 and bit 3 of CR17. Setting bit 3 of CR31 to 1 forces doubleword mode. CR51\_5-4 are extension bits 9-8 of this register.



**Underline Location Register (CR14)**

Read/Write Address: 3?5H, Index 14H

Power-On Default: Undefined

This register specifies the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
= 0	DBW MOD	CNT BY4	UNDERLINE LOCATION				

Bits 4-0 UNDERLINE LOCATION

5-bit Value = (scan line count of a character row on which an underline occurs) - 1

Bit 5 CNT BY4 - Select Count by 4 Mode

0 = The memory address counter depends on bit 3 of CR17 (count by 2)

1 = The memory address counter is incremented every four character clocks

The CNT BY4 bit is used when double word addresses are used.

Bit 6 DBW MOD - Select Doubleword Mode

0 = The memory addresses are byte or word addresses

1 = The memory addresses are doubleword addresses

Bit 7 Reserved = 0

---

**Start Vertical Blank Register (CR15)**

Read/Write Address: 3?5H, Index 15H

Power-On Default: Undefined

This register specifies the scan line at which the vertical blanking period begins.

7	6	5	4	3	2	1	0
START VERTICAL BLANK 7-0							

Bits 7-0 START VERTICAL BLANK 7-0

11-bit value = (scan line count at which BLANK becomes active) - 1.

Bit 8 is CR7\_3. Bit 9 is CR9\_5. Bit 10 is CR5E\_2.

---

**End Vertical Blank Register (CR16)**

Read/Write                      Address: 3?5H, Index 16H

Power-On Default: Undefined

This register specifies the scan line count value when the vertical blank period ends.

7	6	5	4	3	2	1	0
END VERTICAL BLANK							

Bits 7-0            END VERTICAL BLANK

Value = least significant 8 bits of the scan line counter value at which vertical blanking ends

To obtain this value, add the desired width of the vertical blanking pulse in scan lines to [(value in the Start Vertical Blank register)-1], also in scan lines. The 8 least significant bits of this sum are programmed into this field. This allows a maximum vertical blanking pulse of 255 scan line units.

---

**CRTC Mode Control Register (CR17)**

Read/Write                      Address: 3?5H, Index 17H

Power-On Default: 00H

This register is a multifunction control register, with each bit defining a different specification.

7	6	5	4	3	2	1	0
RST	BYT E MOD	ADW 16K	= 0	WD MOD	VT X2	4BK HGC	2BK CGA

Bit 0            2BK CGA - Select Bank 2 Mode for CGA Emulation  
0 = Row scan counter bit 0 is substituted for memory address bit 13 during active display time  
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller

This bit allows memory mapping compatibility with the IBM CGA graphics mode.

Bit 1            4BK HGC - Select Bank 4 Mode for HGA Emulation  
0 = Row scan counter bit 1 is substituted for memory address bit 14 during active display time  
1 = Memory address bit 14 appears on the memory address output bit 14 signal of the CRT controller

The combination of this bit and bit 0 of this register allows compatibility with Hercules HGC graphics memory mapping.

Bit 2            VT X2 - Select Vertical Total Double Mode  
0 = Horizontal retrace clock selected  
1 = Horizontal retrace clock divided by two selected

This bit selects horizontal retrace clock or horizontal retrace clock divided by two as the clock that controls the vertical timing counter. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is double.

Bit 3            WD MOD - Select Word Mode  
0 = Memory address counter is clocked with the character clock input, and byte mode addressing for the video memory is selected  
1 = Memory address counter is clocked by the character clock input divided by 2, and word mode addressing for the video memory is selected

Bit 4            Reserved = 0

Bit 5      ADW 16K - Address Wrap  
0 = When word mode is selected by bit 6 of this register, memory address counter bit 13 appears on the memory address output bit 0 signal of the CRT controller and the video memory address wraps around at 16 KBytes  
1 = When word mode is selected by bit 6 of this register, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRT controller

This bit is useful in implementing IBM CGA mode.

Bit 6      BYTE MODE - Select Byte Addressing Mode  
0 = Word mode shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output  
1 = Byte address mode

Bit 7      RST - Hardware Reset  
0 = Vertical and horizontal retrace pulses always inactive  
1 = Vertical and horizontal retrace pulses enabled

This bit does not reset any other registers or outputs.

---

**Line Compare Register (CR18)**

Read/Write                      Address: 3?5H, Index 18H  
Power-On Default: Undefined

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0. The linear address counter then sequentially addresses the display buffer starting at address 0. Each subsequent row address is determined by the addition of the Offset (CR13) register content.

7	6	5	4	3	2	1	0
LINE COMPARE POSITION 7-0							

Bit 7-0      LINE COMPARE POSITION 7-0  
  
11-bit Value = number of scan lines at which the screen is split into screen A and screen B  
  
Bit 8 is CR7\_4. Bit 9 is CR9\_6. Bit 10 is CR5E\_6.

---

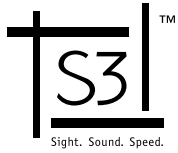
**CPU Latch Data Register (CR22)**

Read Only                              Address: 3?5H, Index 22H  
Power-On Default: Undefined

This register is used to read the CPU latch in the Graphics Controller.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU LATCH - N							

Bits 7-0      GRAPHICS CONTROLLER CPU LATCH - N  
  
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.



**Attribute Index Register (CR24)**

Read Only                      Address: 3?5H, Index 24H, 26H  
Power-On Default: Undefined

This register is used to read the value of the Attribute Controller Index register and its associated internal address flip-flop (AFF). It can be read at either index 24H or 26H.

7	6	5	4	3	2	1	0
AFF	= 0	ENV	ATTRIBUTE CONTROLLER INDEX				

Bits 4-0      ATTRIBUTE CONTROLLER INDEX

This value is the Attribute Controller Index Data at I/O port 3C0H.

Bit 5      ENV- Enable Video Display

This is the setting of bit 5 of 3C0H, indicating video display enabled status (1 = enabled).

Bit 6      Reserved = 0

Bit 7      AFF

Inverted Internal Address flip-flop

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## 2.4 GRAPHICS CONTROLLER REGISTERS

The graphics controller registers are located at a two byte I/O address space. These registers are accessed by first writing an index to the Graphics Address register (at 3CEH) and then accessing the Data register (at 3CFH).

---

### Graphics Controller Index Register

Read/Write                      Address: 3CEH  
Power-On Default: Undefined

This register is loaded with a binary index value that determines which graphics controller register will be accessed. This value is referred to as the "Index Number" of the GR register (GR0-6).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	GR CONT ADDRESS			

Bits 3-0            GR CONT ADDRESS - Graphics Controller Register Index

Value = Index of the register where data is to be accessed.

Bits 7-4            Reserved = 0

---

### Graphics Controller Data Register

Read/Write                      Address: 3CFH  
Power-On Default: Undefined

This register is the data port for the graphics controller register indexed by the Graphics Controller Index register.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER DATA							

Bit 7-0            GRAPHICS CONTROLLER DATA

Value = Data to the Graphics Controller register indexed by the graphics controller address

**Set/Reset Data Register (GR0)**

Read/Write Address: 3CFH, Index 00H

Power-On Default: Undefined

This register represents the value written to all 8 bits of the respective memory plane when the CPU executes a memory write in write modes 0 and 3.

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
= 0	= 0	= 0	= 0	SET/RESET DATA			

Bits 3-0 SET/RESET DATA

Value = the color value for CPU memory write operations

In write mode 0, the set/reset data can be enabled on the corresponding bit of the Enable Set/Reset Data register. In write mode 3, there is no effect on the Enable Set/Reset Data register.

Bits 7-4 Reserved = 0

**Enable Set/Reset Data Register (GR1)**

Read/Write Address: 3CFH, Index 01H

Power-On Default: Undefined

These bits enable the set/reset data, and affect write mode 0.

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
= 0	= 0	= 0	= 0	ENB SET/RST DATA			

Bits 3-0 ENB SET/RST DATA

When each bit is a logical 1, the respective memory plane is written with the value of the Set/Reset Data register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

Bits 7-4 Reserved = 0

**Color Compare Register (GR2)**

Read/Write Address: 3CFH, Index 02H

Power-On Default: Undefined

These bits represent a 4-bit color value to be compared. In read mode 1, the CPU executes a memory read, the read data is compared with this value and returns the results. This register works in conjunction with the Color Don't Care register.

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
= 0	= 0	= 0	= 0	COLOR COMPARE DATA			

Bits 3-0 COLOR COMPARE DATA

Value = reference color used to compare each pixel

Each of the 8-bit positions of the read data are compared across four planes and a logical 1 is returned in each bit position for which the colors match.

Bits 7-4 Reserved = 0

**Raster Operation/Rotate Count Register (GR3)**

Read/Write Address: 3CFH, Index 03H

Power-On Default: Undefined

This register selects a raster operation function and indicates the number of bits the CPU data will be rotated (right) on the video memory write operation.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	RST-OP 1 0		ROTATE-COUNT		

Bits 2-0 ROTATE-COUNT

Value = the number of positions to right-rotate data during a CPU memory write

To write non-rotated data, the CPU must preset a count of 0.

Bits 4-3 RST-OP - Select Raster Operation

00 = No operation

01 = Logical AND with latched data

10 = Logical OR with latched data

11 = Logical XOR with latched data

The data written to memory can operate logically with the data already in the processor latches. This function is not available in write mode 1. The logical function specified by this register is applied to data being written to memory while in modes 0, 2 and 3.

Bits 7-5 Reserved = 0

**Read Plane Select Register (GR4)**

Read/Write Address: 3CFH, Index 04H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	RD-PL-SL 1 0	

Bits 1-0 RD-PL-SL - Read Plane Select

00 = Plane 0

01 = Plane 1

10 = Plane 2

11 = Plane 3

This is the memory plane from which the CPU reads data in read mode 0. These bits have no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored.

Bits 7-2 Reserved = 0

**Graphics Controller Mode Register (GR5)**

Read/Write Address: 3CFH, Index 05H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	SHF-MODE 256 O/E	O/E MAP	RD CMP	= 0	WRT-MD 1 0		

Bit 1-0 WRT-MD - Select Write Mode

These bits select the CPU write mode into video memory. The function of each mode is defined as follows:

00 = Write Mode 0

Each of four video memory planes is written with the CPU data rotated by the number of counts in the rotate register. If the Set/Reset register is enabled for any of four planes, the corresponding plane is written with the data stored in the set/reset register. Raster operations and bit mask registers are effective.

01 = Write Mode 1

Each of four video memory planes is written with the data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, set/reset data, enable set/reset data and bit mask registers are not effective.

10 = Write Mode 2

Memory planes 0-3 are filled with 8 bits of the value of CPU write data bits 0-3, respectively. For example, if write data bit 0 is a 1, eight 1's are written to memory plane 0. The data on the CPU data bus is treated as the color value. The Bit Mask register is effective as the Mask register. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A logical 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored.

11 = Write Mode 3

Each of four video memory planes is written with 8 bits of the color value contained in the set/reset register for that plane. The Enable Set/Reset register is not effective. Rotated CPU write data is ANDed with the bit mask register to form an 8-bit value that performs the same function as the Bit Mask register in write modes 0 and 2. This write mode can be used to fill an area with a single color and pattern

Bit 2 Reserved = 0

Bit 3 RD CMP - Enable Read Compare

0 = The CPU reads data from the video memory planes. The plane is selected by the Read Plane Select register.

This is called read mode 0

1 = The CPU reads the results of the logical comparison between the data in four video memory planes selected by the contents of the Color Don't Care register and the contents of the Color Compare register. The result is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1

Bit 4 O/E MAP - Select Odd/Even Addressing

0 = Standard addressing.

1 = Odd/even addressing mode selected.

When this bit is set to 1, even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3. This option is useful for emulating the CGA compatible mode. The value of this bit should be the inverted value programmed in bit 2 of the Sequencer Memory Mode register (SR4). This bit affects reading of display memory by the CPU.



- Bit 5 SHF-MODE - Select Odd/Even Shift Mode  
 0 = Normal shift mode  
 1 = The video shift registers in the graphics section are directed to format the serial data stream with even-numbered bits from both planes on the even-numbered planes and odd-numbered bits from both planes on the odd planes
- Bit 6 SHF-MODE - Select 256 Color Shift Mode  
 0 = Bit 5 in this register controls operation of the video shift registers  
 1 = The shift registers are loaded in a manner that supports the 256 color mode
- Bit 7 Reserved = 0

---

**Memory Map Mode Control Register (GR6)**

Read/Write Address: 3CFH, Index 06H  
 Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	MEM-MAP		CHN	TXT
				1 0		O/E	/GR

- Bit 0 TXT/GR - Select Text/Graphics Mode  
 0 = Text mode display addressing selected  
 1 = Graphics mode display addressing selected. When set to graphics mode, the character generator address latches are disabled
- Bit 1 CHN O/E - Chain Odd/Even Planes  
 0 = A0 address bit unchanged  
 1 = CPU address bit A0 is replaced by a higher order address bit. The content of A0 determines which memory plan is to be addressed. A0 = 0 selects planes 0 and 2, and A0 = 1 selects planes 1 and 3. This mode can be used to double the address space into video memory
- Bits 3-2 MEM-MAP - Memory Map Mode  
 00 = A0000H to BFFFFH (128 KBytes)  
 01 = A0000H to AFFFFH (64 KBytes)  
 10 = B0000H to B7FFFH (32 KBytes)  
 11 = B8000H to BFFFFH (32 KBytes)
- These bits control the address mapping of video memory into the CPU address space.
- Bits 7-4 Reserved = 0

---

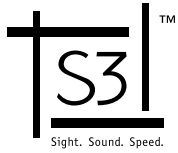
**Color Don't Care Register (GR7)**

Read/Write Address: 3CFH, Index 07H  
 Power-On Default: Undefined

This register is effective in read mode 1, and controls whether the corresponding bit of the Color Compare Register is to be ignored or used for color comparison.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COMPARE PLANE SEL			

- Bits 3-0 COMPARE PLANE SEL - Compare Plane Select  
 0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory performed in read mode 1  
 1 = The corresponding color plane is used for color comparison with the data in the Color Compare register
- Bits 7-4 Reserved = 0



**Bit Mask Register (GR8)**

Read/Write Address: 3CFH, Index 08H  
Power-On Default: Undefined

Any bit programmed to 0 in this register will cause the corresponding bit in each of four memory planes to be immune to change. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bits 7-0 BIT MASK

A logical 0 means the corresponding bit of each plane in memory is set to the corresponding bit in the processor latches. A logical 1 means the corresponding bit of each plane in memory is set as specified by other conditions.

## 2.5 ATTRIBUTE CONTROLLER REGISTERS

The attribute controller registers are located at the same byte I/O address for writing address and data. An internal address flip-flop (AFF) controls the selection of either the attribute index or data registers. To initialize the address flip-flop (AFF), an I/O read is issued at address 3BAH or 3DAH. This presets the address flip-flop to select the index register. After the index register has been loaded by an I/O write to address 3C0H, AFF toggles and the next I/O write loads the data register. Every I/O write to address 3C0H toggles this address flip-flop. However, it does not toggle for I/O reads at address 3C0H or 3C1H. The Attribute Controller Index register is read at 3C0H, and the Attribute Controller Data register is read at address 3C1H.

---

### Attribute Controller Index Register

Read/Write Address: 3C0H  
 Power-On Default: Undefined

This register is loaded with a binary index value that determines which attribute controller register will be accessed. This value is referred to as the "Index Number" of the AR register (AR0-14).

7	6	5	4	3	2	1	0
R	R	ENB PLT	ATTRIBUTE ADDRESS				

Bits 4-0 ATTRIBUTE ADDRESS

Value = Index to the attribute controller register where data is to be written.

Bit 5 ENB PLT - Enable Video Display

0 = Video display access to the palette registers disabled. The Attribute Controller register can be accessed by the CPU

1 = Display video using the palette registers enabled (normal display operation). The palette registers (AR0-ARF) cannot be accessed by the CPU

This bit is effective only in 8-bit modes.

Bits 7-6 Reserved

---

### Attribute Controller Data Register (

Read/Write Address: R: 3C1H/W: 3C0H  
 Power-On Default: Undefined

This register is the data port for the attribute controller register indexed by the Attribute Controller Index register.

7	6	5	4	3	2	1	0
ATTRIBUTE DATA							

Bits 7-0 ATTRIBUTE DATA

Value = Data to the attribute controller register indexed by the attribute controller address

**Palette Registers (AR00-0F)**

Read/Write Address: 3C1H/3C0H, Index 00H-0FH

Power-On Default: Undefined

These are 16, 6-bit registers pointed to by the index and color code. They allow a dynamic mapping between the text attribute or graphics color input and the display color on the CRT screen.

7	6	5	4	3	2	1	0
= 0	= 0	SECONDARY SR SG SB			PRIMARY R G B		

Bits 5-0 PALETTE COLOR

The 6-bit display color, bits 5-0 are output as SR, SG/I, SB/V, R, G and B respectively

Bits 7-6 Reserved = 0

**Attribute Mode Control Register (AR10)**

Read/Write Address: 3C1H/3C0H, Index 10H

Power-On Default: 00H

The contents of this register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
SEL V54	256 CLR	TOP PAN	= 0	ENB BLNK	ENB LGC	MON ATB	TX /GR

Bit 0 TX/GR - Select Graphics Mode  
0 = Selects text attribute control mode  
1 = Selects graphics control mode

This bit must be programmed during screen off (SR1\_5 = 1) or during the vertical retrace period. Setting SR1\_5 to 1 may take up to 3 HSYNCS to take effect.

Bit 1 MON ATB - Select Monochrome Attributes  
0 = Selects color display text attributes  
1 = Selects monochrome display text attributes

Bit 2 ENB LGC - Enable Line Graphics  
0 = The ninth dot of a text character (bit 0 of SR1 = 0) is the same as the background  
1 = Special line graphics character codes enabled

When this bit is set to 1, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0H through DFH. For other characters, the ninth dot is the same as the background.

Bit 3 ENB BLNK - Enable Blinking  
0 = Selects the background intensity for the text attribute input  
1 = Selects blink attribute in text modes

This bit must also be set to 1 for blinking graphics modes. The blinking counter is operated by the vertical retrace counter (VRTC) input. It divides the VRTC input by 32. The blinking rates are ON for 16 VRTC clocks and OFF for 16 VRTC clocks. In the graphics mode, when blink is activated, the most significant color bit (bit 3) for each dot is inverted alternately, thus allowing two different colors to be displayed for 16 VRTC clocks each.

When the cursor is displayed in the text mode, it is blinked at a rate of ON for 8 VRTC clocks and OFF for 8 VRTC clocks (period by 16 frames). The displayed characters are independently blinked at the rate of 32 frames as above.

Bit 4 Reserved = 0

- Bit 5 TOP PAN - Top Panning Enable  
 0 = Line compare has no effect on the output of the pixel panning register  
 1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC occurs in the CRT controller. At the top of screen the output of the Pixel Panning register returns to its programmed value. This bit allows a top portion of a split screen to be panned.
- Bit 6 256 CLR - Select 256 Color Mode  
 0 = 4 bits of video (translated to 6 bits by the palette) are output every internal dot-clock cycle  
 1 = Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot-clock
- Bit 7 SEL V54 - Select V[5:4]  
 0 = In VGA, mode, bits 5-4 of video output are generated by the attribute palette registers. Bits 7-6 of video output are always generated by bits 3-2 of AR14  
 1 = Bits 5-4 of video output are generated by bits 1-0 of AR14

---

**Border Color Register (AR11)**

Read/Write Address: 3C1H/3C0H, Index 11H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
BORDER COLOR							

Bits 7-0 BORDER COLOR

Value = Border color displayed on the CRT screen

The border is an area around the screen display area. This register is only effective in 8-bit modes. See also CR33\_5.

---

**Color Plane Enable Register (AR12)**

Read/Write Address: 3C1H/3C0H, Index 12H  
 Power-On Default: 00H

This register enables the respective video memory color plane 3-0 and selects video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
= 0	= 0	VDT-SEL 1 0		DISPLAY PLANE ENBL			

Bits 3-0 DISPLAY PLANE ENBL

A 0 in any of these bits forces the corresponding color plane bit to 0 before accessing the internal palette. A 1 in any of these bits enables the data on the corresponding color plane.

**Bits 5-4** VDT-SEL - Video Test Select

These bits select two of the eight bit color outputs to be available in the Input Status 1 register. The output color combinations available on the status bits are as follows:

D STS MUX		STS 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Bits 7-6 Reserved = 0

---

**Horizontal Pixel Panning Register (AR13)**

Read/Write Address: 3C1H/3C0H, Index 13H  
 Power-On Default: 00H

This register specifies the number of pixels to shift the display data horizontally to the left. Pixel panning is available in both text and graphics modes. It is not available with Enhanced mode memory mappings (CR31\_3 = 1).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	NUMBER OF PAN SHIFT			

**Bits 3-0** NUMBER OF PAN SHIFT

Value = the number of pixels to shift the display data horizontally to the left

In the 9 pixels/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixels/character text mode and all graphics modes, except 256 color mode, a maximum shift of 7 pixels is possible. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte.

Bits 3-0	Number of pixels shifted in		
	9 pixel/char.	8 pixel/char.	256 color mode
0000	1	0	0
0001	2	1	-
0010	3	2	1
0011	4	3	-
0100	5	4	2
0101	6	5	-
0110	7	6	3
0111	8	7	-
1000	0	-	-

Bits 7-4 Reserved = 0

**Pixel Padding Register (AR14)**

Read/Write Address: 3C1H/3C0H, Index 14H

Power-On Default: 00H

This register specifies the high-order bits of video output when pixel padding is enabled and disabled in the 256 color mode.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	PIXEL PADDING V7 V6 V5 V4			

Bits 1-0 PIXEL PADDING V5, V4

These bits are enabled with a logical 1 of bit 7 of AR10, and can be used in place of the V5 and V4 bits from the Palette registers to form the 8-bit digital color value output.

Bits 3-2 PIXEL PADDING V7, V6

In all modes except 256 color mode, these bits are the two high-order bits of the 8-bit digital color value output.

Bits 7-4 Reserved = 0

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## 2.6 RAMDAC REGISTERS

### DAC Mask Register

Read/Write Address: 3C6H  
Power-On Default: Undefined

The CPU can access this register at any time.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bits 7-0 DAC ADDRESS MASK

The contents of this register are bit-wise logically ANDed with the CLUT address input. This register is initialized to FFH by the BIOS during a video mode set.

### DAC Read Index Register

Write Only Address: 3C7H  
Power-On Default: Undefined

This register contains the pointer to one of 256 palette data registers and is used when reading the color palette.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bits 7-0 DAC READ ADDRESS

Each time the color code is written to this register, it identifies that a read sequence will occur. A read sequence consists of three successive byte reads from the RAMDAC data register at I/O address 3C9H. In 6-bit CLUT mode, the least significant 6 bits of each byte taken from the RAMDAC data register contain the corresponding color value, and the most significant 2 bits contain zeros. The order is red byte first, then green, and finally blue. The sequence of events for a read cycle is:

1. Write the color code to this register (RAMDAC Read Index) at address 3C7H.
2. The contents of the location in the color look-up table pointed to by the color code are transferred to the RAMDAC data register at address 3C9H.
3. Three bytes are read back from the RAMDAC data register.
4. The contents of this register auto-increment by one.
5. Go to step 2.

The effects of writing to the RAMDAC data register during a three-byte read cycle or reading from the RAMDAC data register during a 3-byte write cycle (i.e., interrupting the sequence) are undefined and may change the look-up table contents.



### DAC Status Register

Read Only                      Address: 3C7H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	DAC-STS	

Bits 1-0            DAC-STS - RAMDAC Cycle Status

The last executing cycle was:

00 = Write Palette cycle

11 = Read Palette cycle

Reads from the RAMDAC Write Index at address 3C8H or the DAC status register at address 3C7H do not interfere with read or write cycles and may take place at any time.

Bits 7-2            Reserved = 0

### DAC Write Index Register

Read/Write                      Address: 3C8H

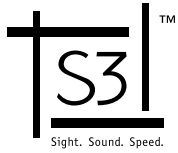
Power-On Default: Undefined

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS							

Bits 7-0            DAC WRITE ADDRESS

This register contains the pointer to one of 256 palette data registers and is used during a palette load. Each time the color code is written to this register, it identifies that a write sequence will occur. A write sequence consists of three successive byte writes to the DAC data register at I/O address 3C9H. In 6-bit CLUT mode, the least significant 6 bits of each byte are shifted up by 2, with two LSB 0's added. The order is red byte first, then green, and finally blue. Once the third byte has been written, the value in the data register is written to the location pointed to by the color code. The sequence of events for a write cycle is:

1. Write the color code to this register (DAC Write Index) at address 3C8H.
2. Three bytes are written to the DAC Data register at address 3C9H.
3. The contents of the DAC data register are transferred to the location in the color look-up table pointed to by the color code.
4. The DAC Write Index register auto-increments by 1.
5. Go to step 2.



**RAMDAC Data Register**

Read/Write Address: 3C9H

Power-On Default: Undefined

This register is a data port to read or write the contents of the location in the color look-up table pointed to by the DAC Read Index or the DAC Write Index registers.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bits 7-0 DAC READ/WRITE DATA

To prevent "snow flicker" on the screen, an application reading data from or writing data to the DAC Data register should ensure that the BLANK input to the RAMDAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals, checking 3?AH\_3) to determine when retrace is occurring, or by using the screen-off bit SR1\_5.

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## Section 3: Extended Sequencer Register Descriptions

In the following register descriptions, R' stands for reserved (write = 0, read = undefined).

### Unlock Extended Sequencer Register (SR8)

Read/Write Address: 3C5H, Index 08H  
 Power-On Default: 00H

Loading xxxx0110b (e.g., 06H) unlocks accessing of all the S3 extensions (SR9 - SRFF) to the standard VGA Sequencer register set. (x = don't care).

7	6	5	4	3	2	1	0
R	R	R	R	=0	=1	=1	=0

### Extended Sequencer 9 Register (SR9)

Read/Write Address: 3C5H, Index 09H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
MMIO-VGA	R	R	R	R	R	R	LAC

Bit 0 LAC - Linear Addressing Control  
 0 = Use VGA logic for linear addressing (memory writes)  
 1 = Bypass VGA logic for linear addressing

Bits 6-1 Reserved

Bit 7 MMIO-VGA - Memory-mapped I/O register + VGA access only  
 0 = When MMIO is enabled, both programmed I/O and memory-mapped I/O register accesses are allowed  
 1 = When MMIO is enabled, only memory-mapped I/O register accesses plus standard VGA I/O port accesses are allowed

PCI04\_0 can be used to disable all I/O accesses, including standard VGA.

**Extended Sequencer D Register (SRD)**

Read/Write Address: 3C5H, Index 0DH

Power-On Default: 00H

This register provides feature connector control and also provides independent control of the HSYNC and VSYNC signals, therefore supporting the VESA DPMS (Display Power Management Control) standard.

7	6	5	4	3	2	1	0
VSY-CTL		HSY-CTL		R=0	R=0	R=0	GPS
1	0	1	0				

Bit 0 GPS - GPOUT Pin State  
 0 = GPOUT pin is driven with logic 0  
 1 = GPOUT pin is driven with logic 1

Bits 3-1 Reserved = 0

Bits 5-4 HSY-CTL - HSYNC Control  
 00 = Normal operation  
 01 = HSYNC = 0  
 10 = HSYNC = 1  
 11 = Reserved

Bits 7-6 VSY-CTL - VSYNC Control  
 00 = Normal operation  
 01 = VSYNC = 0  
 10 = VSYNC = 1  
 11 = Reserved

**MCLK Value Low Register (SR10)**

Read/Write Address: 3C5H, Index 10H

Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR11 generate an MCLK value of 45 MHz. All other MCLK values must be specified by programming of SR10 and SR11. Loading of a new value is enabled by either bit 0 or bit 5 of SR15. After loading any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
R	PLL R VALUE		PLL N-DIVIDER VALUE				

Bits 4-0 PLL N-DIVIDER VALUE

These bits contain the binary equivalent of the integer (1-31) divider used to scale the input to the MCLK PLL.

Bits 6-5 PLL R VALUE

These bits contain the binary equivalent of the integer (1, 2, 4, 8) range value used to scale the output of the MCLK PLL.

Bit 7 Reserved

Extended Sequencer Registers

**MCLK Value High Register (SR11)**

Read/Write Address: 3C5H, Index 11H

Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR10 generate an MCLK value of 45 MHz. All other MCLK values must be specified by programming of SR10 and SR11. Loading of a new value is enabled by either bit 0 or bit 5 of SR15. After loading any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

- Bits 6-0 PLL M-DIVIDER VALUE  
These bits contain the binary equivalent of the integer (1-127) divider used in the feedback loop of the MCLK PLL.
- Bit 7 Reserved

**DCLK Value Low Register (SR12)**

Read/Write Address: 3C5H, Index 12H

Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR13 generate a DCLK value of 25.175 MHz. The default value is automatically placed in this register when bits 3-2 of 3C2H are programmed to 00b. If bits 3-2 of CR2H are programmed to 01b, the appropriate PLL R and PLL N values for a 28.322 MHz DCLK will automatically be placed in this register. All other DCLK values must be specified by programming of SR12, SR13 and SR29 unless SR39\_0 = 1. Loading of a new value is enabled by either bit 1 or bit 5 of SR15 and by setting bits 3-2 of 3C2H to 11b. After loading any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
PLL R VALUE	PLL N-DIVIDER VALUE						

- Bits 5-0 PLL N-DIVIDER VALUE  
  
7-bit Value = the binary equivalent of the integer (1-127) divider used to scale the input to the DCLK PLL. Bit 6 of this value is SR29\_4.
- Bits 7-6 PLL R VALUE  
000 = frequency divider of 1  
001 = frequency divider of 2  
010 = frequency divider of 4  
011 = frequency divider of 8  
100 = frequency divider of 16  
  
The high order bit of this value is SR29\_2.

**DCLK Value High Register (SR13)**

Read/Write Address: 3C5H, Index 13H

Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR12 generate a DCLK value of 25.175 MHz. The default value is automatically placed in this register when bits 3-2 of 3C2H are programmed to 00b. If bits 3-2 of CR2H are programmed to 01b, the appropriate PLL M value for a 28.322 MHz DCLK will automatically be placed in this register. All other DCLK values must be specified by programming of SR12, SR13 and SR29 unless SR39\_0 = 1. Loading of a new value is enabled by either bit 1 or bit 5 of SR15 and by setting bits 3-2 of 3C2H to 11b. After loading any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
PLL M-DIVIDER VALUE							

Bits 7-0 PLL M- DIVIDER VALUE

9-bit Value = the binary coding of the integer (1-511) divider used in the feedback loop of the TV clock PLL. Bit 8 of this value is SR29\_3.

**CLKSYN Control 1 Register (SR14)**

Read/Write Address: 3C5H, Index 14H

Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT DCLK	EXT MCLK	PSEL	CLR CNT	C TEST	EN CNT	MPLL PD	DPLL PD

Bit 0 DPLL PD - Power down DCLK PLL  
0 = DCLK PLL powered  
1 = DCLK PLL powered down

This bit is used for S3 test purposes only.

Bit 1 MPLL PD - Power down MCLK PLL  
0 = MCLK PLL powered  
1 = MCLK PLL powered down

This bit is used for S3 test purposes only.

Bit 2 EN CNT - Enable clock synthesizer counters  
0 = Clock synthesizer counters disabled  
1 = Clock synthesizer counters enabled

This bit is used for S3 test purposes only.

Bit 3 C TEST - Clock Test  
00= Test DCLK  
01 = Test MCLK  
10 = Test AGP clock  
11 = Test ECLK

The high order bit of this field is SR34\_0. These bits are used for S3 test purposes only.

Extended Sequencer Registers

- Bit 4 CLR CNT - Clear clock synthesizer counters  
 0 = No effect  
 1 = Clear the clock synthesizer counters

This bit is used for S3 test purposes only.
- Bit 5 PSEL - Pin function select  
 0 = GPOUT pin functions normally  
 1 = GPOUT pin is tri-stated

Setting this bit to 1 allows the GPOUT pin to act as an MCLK input. This is enabled by setting bit 6 of this register to 1.
- Bit 6 EXT MCLK - External MCLK Select  
 0 = MCLK provided by internal PLL  
 1 = MCLK is input on GPOUT pin

This bit can also be set to 1 at reset via power-on strapping of ROMD1. An external MCLK is only used for S3 test purposes.
- Bit 7 EXT DCLK - External DCLK Select  
 0 = DCLK provided by internal PLL  
 1 = DCLK is input on XIN pin

This bit can also be set to 1 at reset via power-on strapping of ROMA0. An external DCLK is only used for S3 test purposes.

**CLKSYN Control 2 Register (SR15)**

Read/Write Address: 3C5H, Index 15H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
R	DCLK\ INV	CLK LOAD	DCLK/ 2	DCLK OUT	ACLK OUT	DRFQ EN	MFRQ EN

- Bit 0 MFRQ EN - Enable new MCLK frequency load  
 0 = Register bit clear  
 1 = Load new MCLK frequency

When new MCLK PLL values are programmed, this bit can be set to 1 to load these values in the PLL. The loading may be delayed a small but variable amount of time. This bit should be cleared to 0 after loading to prevent repeated loading. Alternately, use bit 5 of this register to produce an immediate load.
- Bit 1 DFRQ EN - Enable new DCLK frequency load  
 0 = Register bit clear  
 1 = Load new DCLK frequency

When new DCLK PLL values are programmed, this bit can be set to 1 to load these values in the PLL. Bits 3-2 of 3C2H must also be set to 11b if they are not already at this value. The loading may be delayed a small but variable amount of time. This bit should be programmed to 1 at power-up to allow loading of the VGA DCLK value and then left at this setting. Use bit 5 of this register to produce an immediate load.
- Bit 2 ACLK OUT - Output internally generated AGPCLK  
 0 = Normal operation  
 1 = ROMD4 pin outputs the internally generated AGPCLK, ROMD5 pin outputs the AGP 2X clock. and ROMD6 outputs the AGP 4X clock.

This is used only for S3 testing.

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Flat Panel Registers

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- Bit 3 DCLK OUT - Output internally generated DCLK or ECLK  
0 = LCLK pin functions normally  
1 = LCLK pin outputs the internally generated DCLK (SR34\_1 = 0) or ECLK (SR34\_1 = 1)
- This is used only for S3 testing.
- Bit 4 DCLK/2 - Divide DCLK by 2  
0 = DCLK unchanged  
1 = Divide DCLK by 2
- This bit must be set to 1 for clock doubled RAMDAC operation.
- Bit 5 CLK LOAD - MCLK, DCLK, ECLK load  
0 = Clock loading is controlled by bits 0 and 1 of this register  
1 = Load MCLK, DCLK and ECLK PLL values immediately
- To produce an immediate MCLK, DCLK and ECLK load, program this bit to 1 and then to 0. Bits 3-2 of 3C2H must also then be programmed to 11b to load the DCLK values if they are not already programmed to this value. This register must never be left set to 1.
- Bit 6 DCLK INV - Invert DCLK  
0 = DCLK unchanged  
1 = Invert DCLK
- Bit 7 Reserved

---

**CLKSYN Test High Register (SR16)**

Read Only Address: 3C5H, Index 16H  
Power-On Default: 00H

This register is reserved for S3 testing of the internal clock synthesizers.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

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**CLKSYN Test Low Register (SR17)**

Read Only Address: 3C5H, Index 17H  
Power-On Default: 00H

This register is reserved for S3 testing of the internal clock synthesizers.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R



**RAMDAC/CLKSYN Control Register (SR18)**

Read/Write Address: 3C5H, Index 18H

Power-On Default: 00H

7	6	5	4	3	2	1	0
CLKx 2	LUT WR	DAC PD	TST BLUE	TST GRN	TST RED	TST RST	TST EN

Bit 0 TST EN - Enable test counter  
0 = RAMDAC test counter disabled  
1 = RAMDAC test counter enabled

This bit is used for S3 test purposes only.

Bit 1 TST RST - Reset test counter  
0 = No effect  
1 = Reset the RAMDAC test counter

This bit is used for S3 test purposes only.

Bit 2 TST RED - Test red data  
0 = No effect  
1 = Place red data on internal data bus

This bit is used for S3 test purposes only.

Bit 3 TST GRN - Test green data  
0 = No effect  
1 = Place green data on internal data bus

This bit is used for S3 test purposes only.

Bit 4 TST BLUE - Test blue data  
0 = No effect  
1 = Place blue data on internal data bus

This bit is used for S3 test purposes only.

Bit 5 DAC PD - RAMDAC power-down  
0 = RAMDAC powered  
1 = RAMDAC powered-down

When the RAMDAC is powered down, the RAMDAC memory retains its data.

Bit 6 LUT WR - LUT write cycle control  
0 = 2 DCLK LUT write cycle (default)  
1 = 1 DCLK LUT write cycle

Bit 7 CLKx2 - Enable clock doubled mode  
0 = RAMDAC clock doubled mode disabled  
1 = RAMDAC clock doubled mode enabled

This bit must be set to 1 when any of the 2 pixels/clock modes is specified in CR67\_7-4. SR15\_4 must also be set to 1.

**Miscellaneous DAC Control Register (SR19)**

Read/Write Address: 3C5H, Index 19H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	RT	R	R	R	VPD	DMS	DLUT

- Bit 0 DLUT - Disable CLUT  
0 = CLUT enabled  
1 = CLUT disabled (powered down)
- Bit 1 DMS - Disable Monitor Sense  
0 = Monitor sense circuit enabled  
1 = Monitor sense circuit disabled (powered down)
- Bit 2 VPD - VREF Power Down  
0 = RAMDAC VREF circuitry powered  
1 = RAMDAC VREF circuitry powered down
- Bits 5-3 Reserved
- Bit 6 RT - RAM Test  
0 = Disable RAM test  
1 = Enable RAM test
- This bit is used for S3 RAMDAC testing.
- Bit 7 Reserved

**Extended Sequencer 1A Register (SR1A)**

Read/Write Address: 3C5H, Index 1AH

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	EIL	R	R	2xS	R	1xS	DI

- Bit 0 DI - DCLK Invert  
0 = No effect  
1 = Invert DCLK for clock doubled 15/16 bits/pixel modes
- Bit 1 1xS – DAC Signature 1x Clock in Bypass Mode Invert  
0 = No inversion  
1 = Invert
- Bit 2 Reserved
- Bit 3 2xS – DAC Signature 2x Clock in Bypass Mode Invert  
0 = No inversion  
1 = Invert
- Bits 5-4 Reserved
- Bit 6 EIL - Enable Internal Latch  
0 = Disable internal latch on XIN input. This setting must be used if the XIN input is driven when both MCLK and DCLK PLLs are powered down  
1 = Enable internal latch for the same conditions as the = 0 value except that the XIN input is not being driven when it is not being used
- Bit 7 Reserved

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Extended Sequencer Registers

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**Extended Sequencer 1B Register (SR1B)**

Read/Write (see bits)      Address: 3C5H, Index 1BH

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	CC	EGC	R	R	R

Bit 2-0      Reserved

Bit 3      EGC - Enable Gamma Correction  
0 = Gamma correction disabled  
1 = Gamma correction enabled

Bit 4      CC - CLUT Configuration  
0 = CLUT configured for 18-bit color data output  
1 = CLUT configured for 24-bit color data output

Bits 6-5      Reserved

Bit 7      DCC - DCLK Control  
0 = DCLK frequency controlled by 3C2\_3-2  
1 = DCLK frequency always comes from SR12, SR13 and SR29.

**Extended Sequencer 1C Register (SR1C)**

Read/Write      Address: 3C5H, Index 1CH

Power-On Default: 00H

7	6	5	4	3	2	1	0
APD	VRP	FBC		AGP 1X CLOCK SKEW			

Bits 3-0      AGP 1X CLOCK SKEW  
0000 = Decrease by 4x minimum skew  
0001 = Decrease by 4x minimum skew  
0010 = Decrease by 4x minimum skew  
0011 = Decrease by 4x minimum skew  
0100 = Decrease by 3x minimum skew  
0101 = Decrease by 2x minimum skew  
0110 = Decrease by 1x minimum skew  
0111 = Decrease by 1x minimum skew  
1000 = No change  
1001 = Increase by 1x minimum skew  
1010 = Increase by 1x minimum skew  
1011 = Increase by 2x minimum skew  
1100 = Increase by 3x minimum skew  
1101 = Increase by 4x minimum skew  
1110 = Increase by 4x minimum skew  
1111 = Increase by 5x minimum skew

See CRB7\_3-0 for AGP 2x clock skew control.

Bits 5-4      FBC - Feedback Clock Input Select  
00 = Standard feedback clock  
01 = Feedback clock with dummy load  
10 = Internal feedback clock  
11 = Internal feedback clock

**Flat Panel Registers**

- Bit 6      VRP - AGP Voltage Regulator Powerdown  
 0 = AGP voltage regulator powered up  
 1 = AGP voltage regulator powered down
- Bit 7      APD - AGP PLL Powerdown  
 0 = AGP PLL normal operation  
 1 = AGP PLL powered down

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**SDCLKR Delay Register (SR1D)**

Read/Write                      Address: 3C5H, Index 1DH  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
PD[63:32] DELAY				PD[31:0] DELAY			

- Bits 3-0      PD[31:0] DELAY
- Value = Delay of SDCLKR input for PD[31:0]
- Each increment from 0 to 15 increases the return clock signal delay by between 0.15 and 0.4 ns. 0H generates no delay; FH generates 15 units delay.
- Bits 7-4      PD[63:32] DELAY
- Value = Delay of SDCLKR input for PD[63:32]
- Each increment from 0 to 15 increases the return clock signal delay by between 0.15 and 0.4 ns. 0H generates no delay; FH generates 15 units delay.

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**DAC Current Control Register (SR27)**

Read/Write                      Address: 3C5H, Index 27H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	BPE	RAMDAC ADJUST		

- Bits 2-0      RAMDAC ADJUST
- These bits are used to adjust the gain of the RAMDAC.
- Bit 3      BPE - BLANK Pedestal Enable  
 0 = Disable BLANK pedestal  
 1 = Enable BLANK pedestal
- Bits 7-4      Reserved

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Extended Sequencer Registers

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**PLL IREF Control Register (SR28)**

Read/Write Address: 3C5H, Index 28H

Power-On Default: 00H

7	6	5	4	3	2	1	0
AGP VCO		AGP IREF		DCLK IREF		MCLK IREF	

Bits 1-0 MCLK IREF

These bits adjust the IREF current of the MCLK PLL.

Bits 3-2 DCLK IREF

These bits adjust the IREF current of the DCLK PLL.

Bits 5-4 AGP CLOCK IREF

These bits adjust the IREF current of the AGP clock PLL.

Bits 7-6 AGP CLOCK VCO

These bits adjust the VCO gain of the AGP clock PLL.

**DCLK PLL Value Overflow Register (SR29)**

Read/Write Address: 3C5H, Index 29H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	DN6	DM8	DR2	R	R

Bits 1-0 Reserved

Bit 2 DR2 - DCLK PLL R Value Bit 2

See the description for SR12.

Bit 3 DM8 - DCLK PLL M Value Bit 8

See the description for SR13.

Bit 4 DN6 - DCLK PLL N Value Bit 6

See the description for SR13.

Bits 7-5 Reserved

**Extended Sequencer 30 Register (SR30)**

Read/Write unless noted Address: 3C5H, Index 30H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	PL	R	PD	PDC	FT

Bit 0 FT - Flat Panel Logic for TV

0 = Normal operation

1 = TV output uses flat panel centering and expansion logic

Flat Panel Registers

- Bit 1      PDC - Panel Detect Control  
0 = Pin N5 is an input  
1 = Pin N5 is an output
  
- This bit must be cleared to 0 for panel detection. See bit 2 of this register.
- Bit 2      PD - Panel Detect (Read only)  
0 = Flat panel not connected  
1 = Flat panel connected
  
- Bit 1 of this register must be cleared to 0 and the appropriate hardware connections made for this bit to be effective.
- Bit 3      Reserved
- Bit 4      PL - Panellink Interface  
0 = 24-bit single clocked data  
1 = 12-bit double clocked data
- Bits 7-5   Reserved

**Extended Sequencer 31 Register (SR31)**

Read/Write                      Address: 3C5H, Index 31H  
Power-On Default: 00H

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
TCP	DCLK VCO	EFP	EFE	ECLK IFEF	ECLK IFEF		STO

- Bit 0      STO - Serial ROM, Flat Panel/Digital TV Output  
0 = Serial ROM pin definition for the multiplexed ROM/flat panel/digital TV pins  
1 = Flat panel/digital TV pin definition for the multiplexed ROM/flat panel/TV pins
  
- In addition, bit 4 of this register must be set to 1 and CRB0\_3 must be 0 for flat panel operation. CRB0\_4 must be 0 for TV operation. CRB0\_2 must be 0 for serial ROM operation.
- Bits 2-1   ECLK IREF
  
- These bits adjust the IREF current of the ECLK PLL.
- Bit 3      EFE - Enable new ECLK frequency load  
0 = Register bit clear  
1 = Load new ECLK frequency
  
- When new ECLK PLL values are programmed, this bit can be set to 1 to load these values in the PLL. The loading may be delayed a small but variable amount of time. This bit should be cleared to 0 after loading to prevent repeated loading. Alternately, use SR15\_5 to produce an immediate load.
- Bit 4      EFP - Enable Flat Panel Operation  
0 = Flat panel operation disabled  
1 = Flat panel operation enabled
- Bits 5-6   DCLK VCO
  
- These bits adjust the VCO gain of the DCLK PLL.
- Bit 7      TCP - TV Clock Phase  
0 = TVCLKR is in phase with TVCLK  
1 = TVCLKR is 180° out of phase with TVCLK

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Extended Sequencer Registers

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**ECLK Value Low Register (SR32)**

Read/Write Address: 3C5H, Index 32H

Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR33 generate an ECLK value of 45 MHz. All other ECLK values must be specified by programming of SR32 and SR33. Loading of a new value is enabled by bit 5 of SR15. After programming any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
R	PLL R VALUE		PLL N-DIVIDER VALUE				

Bits 4-0 PLL N-DIVIDER VALUE

These bits contain the binary equivalent of the integer (1-31) divider used to scale the input to the ECLK PLL.

Bits 6-5 PLL R VALUE

These bits contain the binary equivalent of the integer (1, 2, 4, 8) range value used to scale the output of the ECLK PLL.

Bit 7 Reserved

**ECLK Value High Register (SR33)**

Read/Write Address: 3C5H, Index 33H

Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR32 generate an ECLK value of 45 MHz. All other ECLK values must be specified by programming of SR32 and SR33. Loading of a new value is enabled by bit 5 of SR15. After loading any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

Bits 6-0 PLL M-DIVIDER VALUE

These bits contain the binary equivalent of the integer (1-127) divider used in the feedback loop of the ECLK PLL.

Bit 7 Reserved

**Extended Sequencer 34 Register (SR34)**

Read/Write Address: 3C5H, Index 34H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	RT	R	R	R	R	COS	CTO

Bit 0 CTO - Clock Test Overflow

This is the high order bit of the clock test select. See SR14\_3.

Bit 1 COS - Clock Output Select

0 = Output DCLK on LCLK pin if SR15\_3 = 1

1 = Output ECLK on LCLK pin if SR15\_3 = 1

Bits 7-2 Reserved

**Digital TV Control Register (SR35)**

Read/Write Address: 3C5H, Index 35H

Power-On Default: 00H

7	6	5	4	3	2	1	0
ODS	TOM	TVM		TVCLK DELAY			

Bits 3-0 TVCLK DELAY

Value = Delay in ns of the TVCLK input from an external encoder

Bits 5-4

TVM - TV Encoder Mode

00 = Bt868/869 mode

01 = B[7:0]G[7:4] on rising edge; G[4:0]R[7:0] on falling edge

10 = R[7:0]G[7:4] on rising edge; G[4:0]B[7:0] on falling edge

11 = Reserved

Bit 6

TOM - TV Output Mode (Streams Processor Off)

0 = TV output mode is other than 8 bpp

1 = TV output mode is 8 bpp

This bit is only effective when the Streams Processor is turned off.

Bit 7

ODS - TV Output Data Switch

0 = TV output data is ordered as specified in bits 5-4 of this register

1 = Data ordering specified in bits 5-4 of this register is reversed

For example, if bits 5-4 = 01b and this bit is set to 1, then the output is G[4:0]R[7:0] on rising edge; B[7:0]G[7:4] on falling edge.

**VGA DCLK Value Low Register (SR36) (Rev. B)**

Read/Write Address: 3C5H, Index 36H

Power-On Default: 00H

This register is used instead of SR12 when SR39\_0 = 1. After loading any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
PLL R VALUE		PLL N-DIVIDER VALUE					

Bits 5-0

PLL N-DIVIDER VALUE

7-bit Value = the binary equivalent of the integer (1-127) divider used to scale the input to the DCLK PLL. Bit 6 of this value is SR39\_4.

Bits 7-6

PLL R VALUE

000 = frequency divider of 1

001 = frequency divider of 2

010 = frequency divider of 4

011 = frequency divider of 8

100 = frequency divider of 16

The high order bit of this value is SR39\_2.



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**VGA DCLK Value High 1 Register (SR37) (Rev. B)**

Read/Write Address: 3C5H, Index 37H

Power-On Default: 00H

This register is used instead of SR13 when SR39\_0 = 1 and 3C2\_3-2 = 00b. After loading any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
PLL M-DIVIDER VALUE							

Bits 7-0 PLL M- DIVIDER VALUE

9-bit Value = the binary coding of the integer (1-511) divider used in the feedback loop of the DCLK PLL. Bit 8 of this value is SR39\_3.

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**VGA DCLK Value High 2 Register (SR38) (Rev. B)**

Read/Write Address: 3C5H, Index 38H

Power-On Default: 00H

This register is used instead of SR13 when SR39\_0 = 1 and 3C2\_3-2 = 01b. After loading any PLL value, software must delay at least 1 ms before taking further action.

7	6	5	4	3	2	1	0
PLL M-DIVIDER VALUE							

Bits 7-0 PLL M- DIVIDER VALUE

9-bit Value = the binary coding of the integer (1-511) divider used in the feedback loop of the DCLK PLL. Bit 8 of this value is SR39\_3.

**Extended Sequencer 39 Register (SR39) (Rev. B)**

Read/Write Address: 3C5H, Index 39H

Power-On Default: 00H

7	6	5	4	3	2	1	0
CSP	CCG	PCE	DN6	DM8	DR2	R	VDS

- Bit 0 VDS – VGA DCLK Select  
0 = Use default values for SR12 and SR13 for VGA DCLK PLL programming  
1 = Use SR36 and SR37 for the VGA DCLK PLL values if 3C2\_3-2 = 00b or SR36 and SR38 for the VGA DCLK PLL values if 3C2\_3-2 = 01b.
- Bit 1 Reserved
- Bit 2 DR2 - DCLK PLL R Value Bit 2  
  
See the description for SR36.
- Bit 3 DM8 - DCLK PLL M Value Bit 8  
  
See the description for SR37 and SR38.
- Bit 4 DN6 - DCLK PLL N Value Bit 6  
  
See the description for SR37 and SR38.
- Bit 5 PCE – Pad Compensation Overwrite Enable  
0 = Use automatic feedback code for the pad compensation  
1 = Use CRB6 value for pad compensation
- Bit 6 CCG – New Compensation Code Generation  
0 = Keep the previous/default pad compensation code (1.5V)  
1 = Generate a new feedback code for pad compensation (1.5V)
- Bit 7 CSP – Compensation Sensor Powerdown  
0 = Disable the 1.5V process compensation sensor  
1 = Enable the 1.5V process compensation sensor

## Section 4: Flat Panel Registers

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### Flat Panel Output Control Register (SR3D)

Read/Write Address: 3C5H, Index 3DH  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
PCD	PDD	R	R	CLK DELAY		R	R

Bits 1-0 Reserved

Bits 3-2 CLK DELAY - PANELCLK Output Delay (Rev. B)  
 00 = No delay.  
 01 = Delayed approximately 100 ps  
 10 = Delayed approximately 200 ps  
 11 = Delayed approximately 300 ps

Bit 4 HWC – Hardware Cursor Fix (Rev. C)  
 0 = Normal Rev. B operation  
 1 = Hardware cursor will appear in last five columns of flat panel display

This bit should be set to 1 for flat panel display with the Streams Processor enabled and the primary stream in 15/16 or 32 bpp mode.

Bit 5 Reserved

Bit 6 PDD - PANELD[23:0] Drive Strength  
 0 = 4 mA (8 mA for Rev. B)  
 1 = 8mA (16 mA for Rev. B)

Bit 7 PCD - PANELCLK Drive Strength  
 0 = 8 mA  
 1 = 16 mA

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### Flat Panel Horizontal Compensation 1 Register (SR54)

Read/Write Address: 3C5H, Index 54H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	HCE	GRAPH EXP		TEXT EXP	

Bits 1-0 TEXT EXP - Text Mode Horizontal Expansion  
 00 = Horizontal expansion disabled  
 01 = Horizontal expansion enabled up to a maximum expansion factor of 1.25  
 10 = Reserved  
 11 = Horizontal expansion enabled up to the horizontal panel size. For VGA panels, 9-dot text modes will be forced to 8-dot text modes.

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 800 columns to limit the expansion and eliminate the undesirable visual effects.

Flat Panel Registers

- Bits 3-2      GRAPH EXP - Graphics Mode Horizontal Expansion  
 00 = Horizontal expansion disabled  
 01 = Horizontal expansion enabled up to a maximum expansion factor of 1.25  
 10 = Reserved  
 11 = Horizontal expansion enabled up to the horizontal panel size. For VGA panels, 9-dot text modes will be forced to 8-dot text modes.  
  
 The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 800 columns to limit the expansion and eliminate the undesirable visual effects.
- Bit 4          HCE - Horizontal Centering Enable  
 0 = Horizontal centering disabled  
 1 = Horizontal centering enabled
- Bits 7-5      Reserved

**Flat Panel Horizontal Compensation 2 Register (SR55)**

Read/Write                      Address: 3C5H, Index 55H  
 Power-On Default: 00H

The bits in this register control enabling of horizontal expansion in specific text/graphics modes. They are effective only if text mode horizontal expansion is enabled via SR54\_1-0. Horizontal expansion for all other modes not controlled by these bits is controlled by SR54\_3-0.

7	6	5	4	3	2	1	0
ATHE	R	R	1024C	800C	640C	80C	40C

- Bit 0          40C - 40-character Text Mode Horizontal Expansion Enable  
 0 = Horizontal expansion disabled in 40-character text mode  
 1 = Horizontal expansion enabled in 40-character text mode  
  
 This bit is effective only if text mode horizontal expansion is enabled via SR54\_1-0.
- Bit 1          80C - 80-character Text Mode Horizontal Expansion Enable  
 0 = Horizontal expansion disabled in 80-character text mode  
 1 = Horizontal expansion enabled in 80-character text mode  
  
 This bit is effective only if text mode horizontal expansion is enabled via SR54\_1-0.
- Bit 2          640C - 320/640-column Graphics Mode Horizontal Expansion Enable  
 0 = Horizontal expansion disabled in 320/640-column graphics mode  
 1 = Horizontal expansion enabled in 320/640-column graphics mode  
  
 This bit is effective only if graphics mode horizontal expansion is enabled via SR54\_3-2.
- Bit 3          800C - 800-column Graphics Mode Horizontal Expansion Enable  
 0 = Horizontal expansion disabled in 800-column graphics mode  
 1 = Horizontal expansion enabled in 800-column graphics mode  
  
 This bit is effective only if graphics mode horizontal expansion is enabled via SR54\_3-2.
- Bit 4          1024C - 1024-column Graphics Mode Horizontal Expansion Enable  
 0 = Horizontal expansion disabled in 1024-column graphics mode  
 1 = Horizontal expansion enabled in 1024-column graphics mode  
  
 This bit is effective only if graphics mode horizontal expansion is enabled via SR54\_3-2.
- Bits 6-5      Reserved
- Bit 7          ATHE - Alternate Text Mode Horizontal Expansion  
 0 = Standard text mode horizontal expansion  
 1 = Alternate text mode horizontal expansion  
  
 This bit affects text mode expansion for 800-column or 1024-column panels.

**Flat Panel Vertical Compensation 1 Register (SR56)**

Read/Write Address: 3C5H, Index 56H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	VCE	GRAPH EXP	TEXT EXP		

Bits 1-0 TEXT EXP - Text Mode Vertical Expansion  
 00 = Vertical expansion disabled  
 01 = Vertical expansion enabled up to a maximum of 480 lines  
 10 = Reserved  
 11 = Vertical expansion enabled up to the vertical panel size

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 480 lines to limit the expansion and eliminate the undesirable visual effects.

Bits 3-2 GRAPH EXP - Graphics Mode Vertical Expansion  
 00 = Vertical expansion disabled  
 01 = Vertical expansion enabled up to a maximum of 480 lines  
 10 = Reserved  
 11 = Vertical expansion enabled up to the vertical panel size.

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 480 lines to limit the expansion and eliminate the undesirable visual effects.

Bit 4 VCE - Vertical Centering Enable  
 0 = Vertical centering disabled  
 1 = Vertical centering enabled

This bit is effective only if vertical expansion is enabled via bits 3-2 of this register.

Bits 7-5 Reserved

**Flat Panel Vertical Compensation 2 Register (SR57)**

Read/Write Address: 3C5H, Index 57H

Power-On Default: 00H

This register is used only when flat panel operation is enabled (SR31\_4 = 1). The bits in this register control enabling of vertical expansion in specific text/graphics modes. Vertical expansion for all other modes not controlled by these bits is controlled by SR56\_3-0.

7	6	5	4	3	2	1	0
ATVE	768G	600G	480G	200G	350G	200T	350T

Bit 0 350T - 350-line Text Mode Vertical Expansion Enable  
 0 = Vertical expansion disabled in 350-line text mode  
 1 = Vertical expansion enabled in 350-line text mode

This bit is effective only if text mode vertical expansion is enabled via SR56\_0 = 1 or SR56\_1 = 1.

Bit 1 200T - 200/400-line Text Mode Vertical Expansion Enable  
 0 = Vertical expansion disabled in 200/400-line text mode  
 1 = Vertical expansion enabled in 200/400-line text mode

This bit is effective only if text mode vertical expansion is enabled via SR56\_0 = 1 or SR56\_1 = 1.

Flat Panel Registers

- Bit 2      350G - 350-line Graphics Mode Vertical Expansion Enable  
 0 = Vertical expansion disabled in 350-line graphics mode  
 1 = Vertical expansion enabled in 350-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56\_2 = 1 or SR56\_3 = 1.
- Bit 3      200G - 200/400-line Graphics Mode Vertical Expansion Enable  
 0 = Vertical expansion disabled in 200/400-line graphics mode  
 1 = Vertical expansion enabled in 200/400-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56\_2 = 1 or SR56\_3 = 1.
- Bit 4      480G - 480-line Graphics Mode Vertical Expansion Enable  
 0 = Vertical expansion disabled in 480-line graphics mode  
 1 = Vertical expansion enabled in 480-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56\_2 = 1 or SR56\_3 = 1.
- Bit 5      600G - 600-line Graphics Mode Vertical Expansion Enable  
 0 = Vertical expansion disabled in 600-line graphics mode  
 1 = Vertical expansion enabled in 600-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56\_2 = 1 or SR56\_3 = 1.
- Bit 6      768G - 768-line Graphics Mode Vertical Expansion Enable  
 0 = Vertical expansion disabled in 768-line graphics mode  
 1 = Vertical expansion enabled in 768-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56\_2 = 1 or SR56\_3 = 1.
- Bit 7      ATVE - Alternate Text Mode Vertical Expansion  
 0 = Standard text mode vertical expansion  
 1 = Alternate text mode vertical expansion

This bit affects text mode expansion for 200/400-line text modes for 600-line or 768-line panels.

**Flat Panel Horizontal Border Register (SR58)**

Read Only                      Address: 3C5H, Index 58H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
FP HORIZONTAL BORDER 7-0							

- Bits 7-0      FP HORIZONTAL BORDER 7-0

9-bit Value = (number of character clocks per line from the first pixel column on the flat panel to last pixel column before the start of the video image) + (number of character clocks per line from the first pixel column after the end of the video image to the last pixel column on the flat panel)

Bit 8 of this value is in SR59\_0. This value is valid only when horizontal centering is enabled (SR54\_4 = 1).

---

**Flat Panel Horizontal Expansion Factor Register (SR59)**

Read Only                      Address: 3C5H, Index 59H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	HORIZ EXP FACTOR			R	R	R	HB8

Bit 0                      HB8 - Flat Panel Horizontal Border Bit 8

Bits 7-0 are in SR58.

Bits 3-1                      Reserved

Bits 6-4                      HORIZ EXP FACTOR

000 = panel size &lt; image size

001 = 1 1/8x image size &gt; panel size ≥ image size

010 = illegal

011 = 1 1/4x image size &gt; panel size ≥ 1 1/8x image size

100 = 1 1/2x image size &gt; panel size ≥ 1 1/4x image size

101 = illegal

110 = 2x image size &gt; panel size ≥ 1 1/2x image size

111 = panel size ≥ 2x image size

Bit 7                      Reserved

---

**Flat Panel Vertical Border Register (SR5A)**

Read Only                      Address: 3C5H, Index 5AH

Power-On Default: 00H

7	6	5	4	3	2	1	0
FP VERTICAL BORDER 7-0							

Bits 7-0                      FP VERTICAL BORDER 7-0

9-bit Value = number of scan lines per frame from the first (top) scan line on the flat panel to the last scan line before the start of the video image

Bit 8 of this value is SR5B\_0. This value is valid only when vertical centering is enabled (SR56\_4 = 1)

---

**Flat Panel Vertical Expansion Factor Register (SR5B)**

Read/Write unless noted      Address: 3C5H, Index 5BH

Power-On Default: 00H

7	6	5	4	3	2	1	0
VERT EXP FACTOR			LRI	VCD	VED	VB8	

Bit 0                      VB8 - Flat Panel Vertical Border Bit 8

Bits 7-0 are in SR5A.

Bit 1                      VED - Vertical Expansion Detect (Read Only)

0 = No vertical expansion

1 = Automatic vertical expansion is being done or would be being done if enabled.

This bit is used only for test purposes.

Flat Panel Registers

Bit 2 VCD - Vertical Centering Detect (Read Only)  
 0 = No vertical centering  
 1 = Automatic vertical centering is being done (it must be enabled)

This bit is used only for test purposes.

Bit 3 LRI - Line Repeat Indicator (Read Only)  
 0 = Current scan line will be repeated on the next scan line  
 1 = Current scan line will not be repeated on the next scan line

This bit is used only for test purposes.

Bits 7-4 VERT EXP FACTOR (Read Only)  
 0000 = No expansion (image equal to or larger than panel size)  
 0001 = No expansion (centered if enabled)  
 0010 = Expand 16-line text to 19-line text  
 0011 = Double every fifth line  
 0100 = Double every fourth line  
 0101 = Double every third line  
 0110 = Expand 14-line text to 19-line text  
 0111 = Double every second line  
 1000 = Double every line  
 1001 = Double one line and triple the second, repeat  
 1010 = Double, double, triple, double, triple, repeat  
 1011 = Double, triple, triple, repeat  
 1100 = Double, double, double, triple, repeat  
 1101 = Expand 8-line text to 19-line text (when CR9\_7 = 1)  
 1110 = Triple every line  
 1111 = Quadruple every line

**Flat Panel Display Enable Position Control Register (SR5C)**

Read/Write Address: 3C5H, Index 5CH  
 Power-On Default: Undefined

This register is effective only for Enhanced modes (8 bits/pixel or higher). The BIOS should program this register to 07H on reset.

7	6	5	4	3	2	1	0
R	R	R	R	FPDEC			

Bits 3-0 FPDEC - Flat Panel Display Enable

Value = starting position of the horizontal and vertical display enables

This field should normally be left at 0111b. A smaller value causes the display enables to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the display enables to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Bits 7-4 Reserved



**Flat Panel/CRT Sync Position Control Register (SR5D)**

Read/Write Address: 3C5H, Index 5DH

Power-On Default: Undefined

This register is effective only for Enhanced modes (8 bits/pixel or higher). The BIOS should program this register to 07H on reset.

7	6	5	4	3	2	1	0
R	R	R	R	FP/CRTSC			

Bits 3-0 FP/CRTSC - Flat Panel/CRT Sync

Value = starting position of the horizontal and vertical syncs

This field should normally be left at 0111b. A smaller value causes the syncs to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the syncs to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Bits 7-4 Reserved

**Flat Panel BIOS Scratch 1 Register (SR5E)**

Read/Write Address: 3C5H, Index 5EH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
RESERVED FOR BIOS							

Bits 7-0 RESERVED FOR BIOS

**Flat Panel BIOS Scratch 2 Register (SR5F)**

Read/Write Address: 3C5H, Index 5FH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
RESERVED FOR BIOS							

Bits 7-0 RESERVED FOR BIOS

**Flat Panel Horizontal Total Register (SR60)**

Read/Write Address: 3C5H, Index 60H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL TOTAL 7-0							

Bits 7-0 FP HORIZONTAL TOTAL 7-0

11-bit Value = [number of character clocks in one scan line] - 5

A character clock is always 8 FPSCCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66\_0. Bits 10-9 are SR67\_1-0.

---

**Flat Panel Horizontal Panel Size Register (SR61)**

Read/Write Address: 3C5H, Index 61H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL PANEL SIZE 7-0							

Bits 7-0 FP HORIZONTAL PANEL SIZE 7-0

11-bit Value = [horizontal panel resolution in character clocks] - 1

A character clock is always 8 FPCLKs (FP dot clocks). For example, for a VGA panel with a horizontal resolution of 640, the programmed value would be the binary equivalent of  $[640/8] - 1$ . The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66\_1. Bits 10-9 are SR67\_3-2.

---

**Flat Panel Horizontal Blank Start Register (SR62)**

Read/Write Address: 3C5H, Index 62H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL BLANK START 7-0							

Bits 7-0 FP HORIZONTAL BLANK START 7-0

11-bit Value = character clock counter value at which blanking begins

A character clock is always 8 FPCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66\_2. Bits 10-9 are SR67\_5-4.

---

**Flat Panel Horizontal Blank End Register (SR63)**

Read/Write Address: 3C5H, Index 63H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	FP HORIZONTAL BLANK END 4-0				

Bits 4-0 FP HORIZONTAL BLANK END 4-0

6-bit Value = least significant 6 bits of the character clock counter value at which blanking ends

A character clock is always 8 FPCLKs (FP dot clocks). To obtain this value, add the desired width of the vertical blanking pulse in character clocks to the value in the FP Horizontal Blank Start register, also in character clocks. The 5 least significant bits of this value are programmed into this field. The programmed value is independent of horizontal compensation and applies to all modes. Bit 5 of this value is SR65\_7. If the horizontal blank period is more than 64 character clocks, then SR66\_3 must be set to 1.

Bits 7-5 Reserved

**Flat Panel Horizontal Sync Start Register (SR64)**

Read/Write Address: 3C5H, Index 64H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL SYNC START 7-0							

Bits 7-0 FP HORIZONTAL SYNC START 7-0

11-bit Value = character clock counter value at which the horizontal sync pulse (LP) becomes active

A character clock is always 8 FPSCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66\_4. Bits 10-9 are SR67\_7-6.

**Flat Panel Horizontal Sync End Register (SR65)**

Read/Write Address: 3C5H, Index 65H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
BE5	R	R	FP HORIZONTAL SYNC END 4-0				

Bits 4-0 FP HORIZONTAL SYNC END 4-0

5-bit Value = least significant 5 bits of the character clock counter value at which the horizontal sync pulse (LP) becomes inactive

A character clock is always 8 FPSCLKs (FP dot clocks). To obtain this value, add the desired width of the horizontal sync pulse in character clocks to the value in the FP Horizontal Sync Start register. The 5 least significant bits of this value are programmed into this field. The programmed value is independent of horizontal compensation and applies to all modes. If the horizontal sync period is more than 32 character clocks, SR66\_5 must be set to 1.

Bits 6-5 Reserved

Bit 7 BE5 - FP Horizontal Sync End Bit 5

Bits 4-0 are in this register.

**Flat Panel Horizontal Overflow Register (SR66)**

Read/Write Address: 3C5H, Index 66H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HSE5	HSS8	HBP	HBS8	HPS8	HT8

Bit 0 FP Horizontal Total Bit 8

Bits 7-0 are in SR60.

Bit 1 FP Horizontal Panel Size Bit 8

Bits 7-0 are in SR61.

Bit 2 FP Horizontal Blank Start Bit 8

Bits 7-0 are in SR62.

Flat Panel Registers

- Bit 3      FP Horizontal Blank Period  
0 = Flat panel horizontal blank period is 64 character clocks or less  
1 = Flat panel horizontal blank period is greater than 64 character clocks
  
- See SR 63\_4-0.
- Bit 4      FP Horizontal Sync Start Bit 8
  
- Bits 7-0 are in SR64.
- Bit 5      FP Horizontal Sync Period  
0 = Flat panel horizontal sync period is 32 character clocks or less  
1 = Flat panel horizontal sync period is greater than 32 character clocks
  
- See SR65\_4-0.
- Bits 7-6    Reserved

**Flat Panel Horizontal Overflow 2 Register (SR67)**

Read/Write                      Address: 3C5H, Index 67H  
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FPHT10=9		FPHPS10-9		FPHBS10-9		FPHSS10-9	

- Bits 1-0      FP Horizontal Total Bits 10-9
  
- Bits 7-0 are in SR60. Bit 8 is SR66\_0.
- Bits 3-2      FP Horizontal Panel Size Bits 10-9
  
- Bits 7-0 are in SR61. Bit 8 is SR66\_1.
- Bits 5-4      FP Horizontal Blank Start Bits 10-9
  
- Bits 7-0 are in SR62. Bit 8 is SR66\_2.
- Bits 7-6      FP Horizontal Sync Start Bits 10-9
  
- Bits 7-0 are in SR64. Bit 8 is SR66\_4.

**Flat Panel Vertical Total Register (SR68)**

Read/Write                      Address: 3C5H, Index 68H  
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL TOTAL 7-0							

- Bits 7-0      FP VERTICAL TOTAL 7-0
  
- 11-bit Value = [number of scan lines from one vertical sync pulse (FLM) active to the next vertical sync pulse active] - 2
  
- The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6E\_2-0.

**Flat Panel Vertical Panel Size Register (SR69)**

Read/Write Address: 3C5H, Index 69H

Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL PANEL SIZE 7-0							

Bits 7-0 FP VERTICAL PANEL SIZE 7-0

11-bit Value = [vertical panel resolution in scan lines] - 1

For example, for a VGA panel with a vertical resolution of 480, the programmed value would be the binary equivalent of 480 - 1. The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6E\_6-4.

**Flat Panel Vertical Blank Start Register (SR6A)**

Read/Write Address: 3C5H, Index 6AH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL BLANK START 7-0							

Bits 7-0 FP VERTICAL BLANK START 7-0

11-bit Value = scan line counter value at which blanking begins

The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6F\_2-0.

**Flat Panel Vertical Blank End Register (SR6B)**

Read/Write Address: 3C5H, Index 6BH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL BLANK END 7-0							

Bits 7-0 FP VERTICAL BLANK END 7-0

Value = least significant 8 bits of the scan line counter value at which blanking ends

To obtain this value, add the desired width of the vertical blanking pulse in scan lines to the value in the FP Vertical Blank Start register, also in scan lines. The 8 least significant bits of this value are programmed into this field. The programmed value is independent of vertical compensation and applies to all modes.

**Flat Panel Vertical Sync Start Register (SR6C)**

Read/Write Address: 3C5H, Index 6CH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL SYNC START 7-0							

Bits 7-0 FP VERTICAL SYNC START 7-0

11-bit Value = [scan line counter value at which the vertical sync pulse (FLM) becomes active] -1

The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6F\_6-4.

**Flat Panel Vertical Sync End Register (SR6D)**

Read/Write Address: 3C5H, Index 6DH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	R	FP VERTICAL SYNC END 3-0			

Bits 3-0 FP VERTICAL SYNC END 3-0

4-bit Value = least significant 4 bits of the character clock counter value at which the vertical sync pulse (FLM) becomes inactive

To obtain this value, add the desired width of the vertical sync pulse in scan lines to the value in the FP Vertical Sync Start register, also in scan lines. The 4 least significant bits of this value are programmed into this field. The programmed value is independent of vertical compensation and applies to all modes.

Bits 7-4 Reserved

**Flat Panel Vertical Overflow 1 Register (SR6E)**

Read/Write Address: 3C5H, Index 6EH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	VPS10-8		R	VT10-8			

Bits 2-0 VT10-8 - FP Vertical Total Bits 10-8

Bits 7-0 are in SR68.

Bit 3 Reserved

Bits 6-4 VPS10-8 - FP Vertical Panel Size Bits 10-8

Bits 7-0 are in SR69.

Bit 7 Reserved

**Flat Panel Vertical Overflow 2 Register (SR6F)**

Read/Write                      Address: 3C5H, Index 6FH  
 Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	VSS10-8			R	VBS10-8		

Bits 2-0            VBS10-8 - FP Vertical Blank Start Bits 10-8

Bits 7-0 are in SR6A.

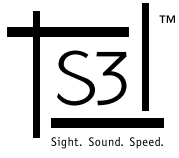
Bit 3                Reserved

Bits 6-4            VSS10-8 - FP Vertical Sync Start Bits 10-8

Bits 7-0 are in SR6C.

Bit 7                Reserved

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## Section 5: Extended CRTC Register Descriptions

These registers are located in CRT Controller address space at locations not used by the VGA standard. All registers are read/write protected at power-up by hardware reset. In order to read/write these registers, CR38 and/or CR39 must be loaded with a changed key pattern (see the register description). The registers will remain unlocked until the key pattern is reset by altering a significant bit.

In the following register descriptions, 'R' stands for reserved (write =0, read = undefined).

---

### Synchronization 0 Register (CR21)

Read/Write Address: 3?5H, Index 23H  
 Power-On Default: 00H

A5H must be programmed into CR39 to access this register.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	DPL	R

Bit 0 Reserved  
 Bit 1 DPL - Delay Primary Stream Display Start Address Load  
 0 = Normal operation  
 1 = Delay PS display start address load by 2 character clocks  
 Bits 7-2 Reserved

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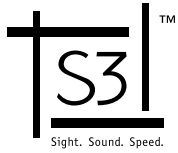
### Synchronization 1 Register (CR23)

Read/Write Address: 3?5H, Index 23H  
 Power-On Default: 00H

This register must be 00H before CR26 is written. For this to be effective, A5H must first be programmed into CR39.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved



Extended CRTC Registers

**Synchronization 2 Register (CR26)**

Read/Write Address: 3?5H, Index 26H

Power-On Default: 00H

The BIOS must write 00H to this register upon each mode set (assuming CR23 is at its default value of 00H). Drivers should write 00H to this register after writing 00H to CR23 before enabling Streams Processor operation. For this to be effective, A5H must first be programmed into CR39.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved

**Device ID High Register (CR2D)**

Read Only Address: 3?5H, Index 2DH

Power-On Default: 8AH

This register should contain the same value as the upper byte of the PCI Device ID (Index 02H) register.

7	6	5	4	3	2	1	0
CHIP ID HIGH							

Bits 7-0 CHIP ID HIGH

Value = 8AH (hardwired)

**Device ID Low Register (CR2E)**

Read Only Address: 3?5H, Index 2EH

Power-On Default: See Below

7	6	5	4	3	2	1	0
CHIP ID LOW							

Bits 7-0 CHIP ID LOW

Value = 22H (hardwired)

**Revision Register (CR2F)**

Read Only Address: 3?5H, Index 2FH

Power-On Default: xxH

7	6	5	4	3	2	1	0
REVISION LEVEL							

Bits 7-0 REVISION LEVEL

Value = xx (hardwired)

The "xx" will change with each revision of the chip.

Extended CRTC Registers

**Old Chip ID Register (CR30)**

Read Only                      Address: 3?5H, Index 30H

Power-On Default: E1H

Use CR2D, CR2E and CR2F for chip ID information.

7	6	5	4	3	2	1	0
OLD ID							

Bits 7-0            OLD ID

value = E1H (hardwired)

**Memory Configuration Register (CR31)**

Read/Write                      Address: 3?5H, Index 31H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	HST DFF	R	R	ENH MAP	VGA 16B	SCRN 2.PG	CPUA BASE

Bit 0            CPUA BASE - Enable Base Address Offset  
 0 = Address offset bits (CR6A\_6-0) are disabled  
 1 = Address offset bits (CR6A\_6-0) are enabled

Setting this bit allows access to up to 8 MBytes of display memory through a 64K window at A0000H.

Bit 1            SCRN 2.PG - Enable Two-Page Screen Image  
 0 = Normal Mode  
 1 = Enable 2K x 1K x 4 map image screen for 1024 x 768 or 800 x 600 screen resolution, or 2K x 512 x 8 map image screen for 640 x 480 screen resolution

Bit 2            VGA 16B - Enable VGA 16-bit Memory Bus Width  
 0 = 8-bit memory bus operation  
 1 = Enable 16-bit bus VGA memory read/writes

This is useful in VGA text modes when VGA graphics controller functions are typically not used.

Bit 3            ENH MAP - Use Enhanced Mode Memory Mapping  
 0 = Force IBM VGA mapping for memory accesses  
 1 = Force 2D Enhanced Mode mappings

Setting this bit to 1 overrides the settings of bit 6 of CR14 and bit 3 of CR17 and causes the use of doubleword memory addressing mode. Also, the function of bits 3-2 of GR6 is overridden with a fixed 64K map at A0000H.

Bits 5-4            Reserved

Bit 6            HST DFF - Enable High Speed Text Display Font Fetch Mode  
 0 = Normal font access mode  
 1 = Enable high speed text display

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz. See bit 5 of CR3A.

Bit 7            Reserved

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Extended CRTC Registers

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**Backward Compatibility 1 Register (CR32)**

Read/Write Address: 3?5H, Index 32H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	VGA FXPG	R	INT EN	R=0	R	R	R

Bits 2-0 Reserved

Bit 3 Reserved = 0

This bit should never be set to 1.

Bit 4 INT EN - Interrupt Enable  
0 = All interrupt generation disabled  
1 = Interrupt generation enabled

Bit 5 Reserved

Bit 6 VGA FXPG - Use Standard VGA Memory Wrapping  
0 = Memory accesses extending past a 256K boundary do not wrap  
1 = Memory accesses extending past a 256K boundary wrap at the boundary

The standard 256K VGA memory page always ends on a natural 256K boundary and accesses beyond this boundary will wrap. If the starting address is moved via bits 4-0 of CR69 (or bits 5-4 of CR31 and bits 1-0 of CR51), the 256K page may not end on a 256K boundary and accesses past the boundary will not wrap. This is the case when this bit is cleared to 0. For standard VGA compatibility when the page base address is moved, this bit is set to 1 to cause wrapping at a 256K boundary.

Bit 7 Reserved

---

**Backward Compatibility 2 Register (CR33)**

Read/Write Address: 3?5H, Index 33H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	LOCK PLTW	BDR SEL	LOCK DACW	-DCK	R	DIS VDE	R

Bit 0 Reserved

Bit 1 DIS VDE - Disable Vertical Display End Extension Bits Write Protection  
0 = VDE protection enabled  
1 = Disables the write protect setting of the bit 7 of CR11 on bits 1 and 6 of CR7

Bit 2 Reserved

Bit 3 -DCK - DCLK Inverted  
0 = DCLK is divided by 2 for 4 bits/pixel modes (see bit 6 of AR10 or bit 4 of CR3A) or is the internal DCLK  
1 = DCLK inverted

Bit 4 LOCK DACW - Lock RAMDAC Writes  
0 = Enable writes to RAMDAC registers  
1 = Disable writes to RAMDAC registers

Bit 5 BDR SEL - Blank/Border Select  
0 = BLANK active time is defined by CR2 and CR3  
1 = BLANK is active during entire display inactive period (no border)

Bit 6 LOCK PLTW - Lock Palette/Border Color Registers  
0 = Unlock Palette/Border Color registers  
1 = Lock Palette/Border Color registers

Bit 7 Reserved

Extended CRTC Registers

**Backward Compatibility 3 Register (CR34)**

Read/Write Address: 3?5H, Index 34H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	ENB SFF	R	PCI RET	PCI ABT	PCI SNP

- Bit 0      PCI SNP - PCI DAC snoop method  
0 = Handling of PCI master aborts and retries during DAC cycles controlled by bits 1 and 2 of this register  
1 = PCI master aborts and retries are not handled during DAC cycles
  
- Bit 1      This bit applies only to PCI designs (not AGP).  
PCI ABT - PCI master aborts during DAC cycles  
0 = PCI master aborts handled during DAC cycles  
1 = PCI master aborts not handled during DAC cycles
  
- Bit 2      Bit 0 of this register must be cleared to 0 for this bit to be effective. This bit applies only to PCI designs (not AGP).  
PCI RET - PCI retries during DAC cycles  
0 = PCI retries handled during DAC cycles  
1 = PCI retries not handled during DAC cycles
  
- Bit 3      Bit 0 of this register must be cleared to 0 for this bit to be effective. This bit applies only to PCI designs (not AGP).  
Reserved
  
- Bit 4      ENB SFF - Enable Start Display FIFO Fetch Register  
0 = Start Display FIFO Fetch register (CR3B) disabled  
1 = Start Display FIFO Fetch register (CR3B) enabled
  
- Bits 7-5    Reserved

**CRT Register Lock Register (CR35)**

Read/Write Address: 3?5H, Index 35H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	LOCK HTMG	LOCK VTMG	R	R	R	R

- Bits 3-0    Reserved
  
- Bit 4      LOCK VTMG - Lock Vertical Timing Registers  
0 = Vertical timing registers are unlocked  
1 = The following vertical timing registers are locked:  
CR6  
CR7 (bits 7,5,3,2,0)  
CR9 (bit 5)  
CR10  
CR11 (bits 3-0)  
CR15  
CR16  
CR6, CR7 registers are also locked by bit 7 of the Vertical Retrace End register (CR11).

Extended CRTC Registers

Bit 5 LOCK HTMG - Lock Horizontal Timing Registers  
 0 = Horizontal timing registers are unlocked  
 1 = The following horizontal timing registers are locked:

- CR00
- CR1
- CR2
- CR3
- CR4
- CR5
- CR17 (bit 2)

All these registers (except bit 2 of CR17) are also locked by bit 7 of the Vertical Retrace End register (CR11).

Bit 7-6 Reserved

**Configuration 1 Register (CR36)**

Read/Write Address: 3?5H, Index 36H  
 Power-On Default: Depends on Strapping

If a pin is identified for a bit in this register, the state of that pin is latched at reset. These pins have internal pull-downs and their states are inverted before being latched, so these bits will default to 1 if the corresponding pin is not pulled up externally. If a pin is not associated with a bit, that bit always defaults to 1 at reset. Other configuration bits are found in CR37. These bits can be accessed only after A5H is written to CR39.

7	6	5	4	3	2	1	0
MEM SIZE		IOD	BP	APB	MCS	PI	

Bit 0 PI - PCI Interrupt (ROMD0 pin)  
 0 = PCI register at offset 3DH reads 00H (no interrupt claimed)  
 1 = PCI register at offset 3DH reads 01H (INTA used as interrupt pin)

Bit 1 MCS - Memory Clock Select (ROMD1 pin)  
 0 = Use external MCLK on GPOUT pin  
 1 = Use internal MCLK

The invert of this bit and SR14\_6 are ORed. This is used only for S3 testing.

Bit 2 APB - AGP PLL Test Mode (ROMD2 pin)  
 0 = AGP PLL test mode (S3 testing only)  
 1 = Normal operation

Bit 3 BP - BIOS Programmability (ROMD3 pin)  
 0 = BIOS ROM is programmable  
 1 = BIOS ROM is not programmable

Bit 4 IOD - I/O Disable (ROMD4 pin)  
 0 = Disable I/O accesses (PCI04\_0 ignored)  
 1 = I/O access controlled via PCI04\_0

Bits 7-5 MEM SIZE  
 000 = 2 MBytes  
 001 = 4 MBytes (except 8 MBytes for 4 bank 2Mx32 SDRAM – Rev. B)  
 010 = 8 MBytes  
 011 = 12 MBytes  
 100 = 16 MBytes  
 101 = 32 MBytes  
 110 = Reserved  
 111 = 32 MBytes for 4 bank 2Mx32 SDRAM – Rev. B

These bits are programmed by the BIOS after boot up.

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Extended CRTC Registers

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**Configuration 2 Register (CR37)**

Read/Write Address: 3?5H, Index 37H

Power-On Default: Depends on Strapping

If a pin is identified for a bit in this register, the state of that pin is latched at reset. These pins have internal pull-downs and their states are inverted before being latched, so these bits will default to 1 if the corresponding pin is not pulled up externally. If a pin is not associated with a bit, that bit always defaults to 1 at reset. Other configuration bits are found in CR36. These bits can be accessed only after A5H is written to CR39.

7	6	5	4	3	2	1	0
ACLK	AGP	AI	ECS	CS	SIDS	NT	ST

- Bit 0 ST - Static Idd Test (ROMD5 pin - S3 testing only)  
0 = Static Idd test enabled  
1 = Normal operation (default)
- Bit 1 NT- NAND Tree Test (ROMD6 pin)  
0 = NAND tree test  
1 = Normal operation
- Bit 2 SIDS - Subsystem ID Source (ROMD7 pin)  
0 = Read subsystem ID information from CR81-CR84  
1 = Read subsystem ID information from BIOS ROM
- Bit 3 CS - Clock Select (ROMA0 pin)  
0 = Use external DCLK on XIN pin, AGP 2x clock on SDCLKOUT pin (Rev. B) (S3 testing)  
1 = Use internal clocks
- Bit 4 ECS - ECLK Select (ROMA1 pin)  
0 = Use external ECLK on GOP0 pin and AGP 4x clock on VIPCLK pin (Rev. B) (S3 testing)  
1 = Use internal clocks
- Bit 5 AI - AGP IDSEL (ROMA2 pin)  
0 = IDSEL connected internally to AD16 (add-in card)  
1 = IDSEL connected internally to AD17 (motherboard)
- Bit 6 AGP - AGP Select (ROMA3 pin)  
0 = PCI protocol used  
1 = AGP protocol used
- Bit 7 ACLK - AGP Clock Select (ROMA4 pin) (Rev. B)  
0 = 1x AGP clock comes from bypass output  
1 = 1x AGP clock comes from AGP PLL output

---

**Register Lock 1 Register (CR38)**

Read/Write Address: 3?5H, Index 38H

Power-On Default: 00H

Loading 01xx10xx (e.g., 48H) into this register unlocks the extended CRTC register set from 20H to 3FH for read/writes. (x = don't care)

7	6	5	4	3	2	1	0
= 0	= 1			= 1	= 0		

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Extended CRTC Registers

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**Register Lock 2 Register (CR39)**

Read/Write Address: 3?5H, Index 39H

Power-On Default: 00H

Loading 101xxxx (e.g., A0H) unlocks the CRTC extension registers from 40H to FFH for reading/writing (x = don't care). Loading A5H allows CR36, CR37, CR68 and CR6F to be written.

7	6	5	4	3	2	1	0
= 1	= 0	= 1					

**Miscellaneous 1 Register (CR3A)**

Read/Write Address: 3?5H, Index 3AH

Power-On Default: 00H

7	6	5	4	3	2	1	0
PCIRB DISA	R	HST DFW	ENH 256	TOP MEM	R	REFRESH CONTROL	

Bits 1-0

REFRESH CONTROL

00 = Use DRAM auto refresh

01 = 1 refresh cycle per horizontal line

10 = 2 refresh cycles per horizontal line

11 = 3 refresh cycles per horizontal line

CR87\_5-4 must also be set properly to control memory refresh.

Bit 2

Reserved

Bit 3

TOP MEM - Enable Top of Memory Access

0 = Top of memory access disabled

1 = Simultaneous VGA text and Enhanced modes are enabled. CPU and CRTC accesses are then directed to the top 32- or 64-KByte area of display memory depending on whether address bit 13 is 0 or 1 respectively.

Bit 4

ENH 256 - Enable 8 Bits/Pixel or Greater Color Enhanced Mode (2D only)

0 = Attribute controller shift registers configured for 4-bit modes

1 = Attribute controller shift register configured for 8-, 16- and 24/32-bit color 2D Enhanced modes

Bit 5

HST DFW - Enable High Speed Text Font Writing

0 = Disable high speed text font writing

1 = Enable high speed text font writing

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz. See bit 6 of CR31.

Bit 6

Reserved

Bit 7

PCIRB DISA - PCI Read Bursts Disabled

0 = PCI read burst cycles enabled

1 = PCI read burst cycles disabled

**Note:** Bit 7 of CR66 must be set to 1 before this bit is set to 1. This bit does not apply to AGP operation.



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Extended CRTC Registers

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**Start Display FIFO Fetch Register (CR3B)**

Read/Write                      Address: 3?5H, Index 3BH  
Power-On Default: 00H

This value must lie in the horizontal blanking period and is typically 5 less than the value programmed in CR0. This parameter helps to ensure that adequate time is available during horizontal blanking for activities such as RAM refresh that require control of the display memory. This register must be enabled by setting bit 4 of CR34 to 1. When the Streams Processor is enabled, FIFO fetching starts at a fixed point based on an internal signal and this register is not effective.

7	6	5	4	3	2	1	0
START DISPLAY FIFO FETCH 7-0							

Bits 7-0            START DISPLAY FIFO FETCH 7-0  
11-bit value = the time in character clocks from the active display start until the restart of fetching of FIFO data after the start of horizontal blanking.

Bit 8 of this value is CR5D\_6. Bits 10-9 of this value are CR5B\_3-2.

---

**Interlace Retrace Start Register (CR3C)**

Read/Write                      Address: 3?5H, Index 3CH  
Power-On Default: 00H

This value allows determination of the even/odd row active display starting positions when operating in an interlaced mode. This register is enabled by bit 5 of CR42.

7	6	5	4	3	2	1	0
INTERLACE RETRACE START POSITION							

Bits 7-0            INTERLACE RETRACE START POSITION  
10-bit Value = offset in terms of character clocks for Interlaced mode start/end in even/odd frames.

Bits 9-8 are CR5B\_1-0.

---

**Software Reset Register (CR3F)**

Read/Write                      Address: 3?5H, Index 3FH  
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	ML	ME	3D	AGP	PCI	MIU

Bit 0            MIU - Memory Interface Software Reset  
0 = Memory interface software reset inactive  
1 = Memory interface software reset active

Bit 1            PCI - PCI Master Software Reset  
0 = PCI master software reset inactive  
1 = PCI master software reset active

Bit 2            AGP - AGP Master Software Reset  
0 = AGP master software reset inactive  
1 = AGP master software reset active

Bit 3            3D - 3D Engine Software Reset  
0 = 3D Engine software reset inactive  
1 = 3D Engine software reset active

**Extended CRTC Registers**

- Bit 4      ME - Master Engine Unit Software Reset  
0 = Master Engine software reset inactive  
1 = Master Engine software reset active
- Bit 5      ML - Motion Compensation/LPB Software Reset  
0 = Motion compensation/LPB software reset inactive  
1 = Motion compensation/LPB software reset active
- Bits 7-6    Reserved

---

**System Configuration Register (CR40)**

Read/Write (See bits)      Address: 3?5H, Index 40H  
Power-On Default: 00H

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
R	R	R	R	R	R	R	E2A

- Bit 0      E2A - Enable 2D Engine Register I/O Access  
0 = 2D Engine register I/O access disabled  
1 = 2D Engine register I/O access enabled

This bit is used only for S3 testing.

- Bits 7- 1    Reserved

---

**BIOS Flag Register (CR41)**

Read/Write      Address: 3?5H, Index 41H  
Power-On Default: 00H

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
BIOS FLAG							

- Bits 7-0      BIOS FLAG

Used by the video BIOS.

---

**Mode Control Register (CR42)**

Read/Write      Address: 3?5H, Index 42H  
Power-On Default: 00H

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
R	R	INTL MOD E	R	R	R	R	D2

- Bit 0      D2  
0 = PCI power management D2 state disabled  
1 = PCI power management D2 state enabled

When this bit is cleared to 0, PCI configuration state writes to enable the D2 power management state (PCIE0\_1-0 = 10b) are ignored.

- Bits 4-1      Reserved

Extended CRTC Registers

Bit 5 INTL MODE - Interlaced Mode  
 0 = Noninterlaced  
 1 = Interlaced

This bit enables the function of CR3C.

Bits 7-6 Reserved

**Extended Mode Register (CR43)**

Read/Write Address: 3?5H, Index 43H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
HCTR X2	R	R	R	R	R	R	R

Bits 6-0 Reserved

Bit 7 HCTR X2 - Horizontal Counter Double Mode  
 0 = Disable horizontal counter double mode  
 1 = Enable horizontal counter double mode (horizontal CRT parameters are doubled)

**Hardware Graphics Cursor Mode Register (CR45)**

Read/Write Address: 3?5H, Index 45H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	HWGC 1280	R	CU	R	HWGC ENB

Bit 0 HWGC ENB - Hardware Graphics Cursor Enable  
 0 = Hardware graphics cursor disabled in any mode  
 1 = Hardware graphics cursor enabled in Enhanced mode

Bit 1 Reserved

Bit 2 CU - Cursor Update  
 0 = The last cursor update made during a frame is effective  
 1 = Only the first cursor update made during a frame is effective

Bit 3 Reserved

Bit 4 HWGC 1280 - Hardware Cursor Right Storage  
 0 = Function disabled  
 1 = For 4 bits/pixel, the last 256 bytes in each 1-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. For 8 bits/pixel, the last 512 bytes in each 2-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. In either case, bits 1-0 of CR4D must be 11b.

Bits 7-5 Reserved

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Extended CRTC Registers

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**Hardware Graphics Cursor Origin-X Registers (CR46, CR47)**

Read/Write Address: 3?5H, Index 46H, 47H

Power-On Default: 0000H

The high order three bits are written into CR46 and the low order byte is written into CR47.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG X (H)			HWGC ORG X (L)							

Bits 10-0 HWGC ORG X(H) (L) - X-Coordinate of Cursor Left Side

Bits 15-11 Reserved

---

**Hardware Graphics Cursor Origin-Y Registers (CR48, CR49)**

Read/Write Address: 3?5H, Index 48H, 49H

Power-On Default: Undefined

The high order three bits are written into CR48 and the low order byte is written into CR49.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG Y (H)			HWGC ORG Y (L)							

Bits 10-0 HWGC ORG Y (H)(L) - Y-Coordinate of Cursor Upper Line

The cursor X, Y position is registered upon writing HWGC ORG Y (H).

Bits 15-11 Reserved

---

**Hardware Graphics Cursor Foreground Color Stack Register (CR4A)**

Read/Write Address: 3?5H, Index 4AH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR FOREGROUND STACK (0-3)							

Bits 7-0 TRUE COLOR FOREGROUND STACK (0-3)

Four foreground color registers are stacked at this address. The stack pointer (common with CR4B) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4A) increments the stack pointer by 1. 8-bit color with single clocking requires 1 write. For 2x clocking, the color for the first pixel clocked out is programmed in register 0 and the color for the second pixel clocked out is programmed in register 1. 15/16-bit color with single clocking requires 2 writes. For 2x clocking, the color for the first pixel clocked out is programmed in registers 0 and 1 and the color for the second pixel clocked out is programmed in registers 3 and 4. 24-bit color requires 3 writes.

Extended CRTC Registers

**Hardware Graphics Cursor Background Color Stack Register (CR4B)**

Read/Write Address: 3?5H, Index 4BH  
 Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR BACKGROUND STACK (0-3)							

Bits 7-0 TRUE COLOR BACKGROUND STACK (0-3)

Four foreground color registers are stacked at this address. The stack pointer (common with CR4B) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4B) increments the stack pointer by 1. 8-bit color with single clocking requires 1 write. For 2x clocking, the color for the first pixel clocked out is programmed in register 0 and the color for the second pixel clocked out is programmed in register 1. 15/16-bit color with single clocking requires 2 writes. For 2x clocking, the color for the first pixel clocked out is programmed in registers 0 and 1 and the color for the second pixel clocked out is programmed in registers 3 and 4. 24-bit color requires 3 writes.

**Hardware Graphics Cursor Storage Start Address Registers (CR4C, CR4D)**

Read/Write Address: 3?5H, Index 4CH, 4DH  
 Power-On Default: Undefined

The high order four bits are written into CR4C and the low order byte is written into CR4D. 10 LSB 0's are added to the address by the hardware.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	HWGC STA(H)							HWGC STA(L)							R	R

Bits 1-0 Reserved = 0 (4K alignment)  
 Bits 14-2 HWGC STA(H)(L) - Hardware Graphics Cursor Storage Start Address  
 Bit 15 Reserved

**Hardware Graphics Cursor Pattern Display Start X-PXL-Position Register (CR4E)**

Read/Write Address: 3?5H, Index 4EH  
 Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START X-POS					

Bits 5-0 HWGC PAT DISP START X-POS - HWGC Pattern Display Start-X Pixel Position  
 This value is the offset (in pixels) from the left side of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the left border of the display.  
 Bits 7-6 Reserved

**Hardware Graphics Cursor Pattern Disp Start Y-PXL-Position Register (CR4F)**

Read/Write Address: 3?5H, Index 4FH

Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START Y-POS					

Bits 5-0 HWGC PAT DISP START Y-POS - HWGC Pattern Display Start-Y Pixel Position

This value is the offset (in pixels) from the top of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the top of the display.

Bits 7-6 Reserved

**Extended System Control 1 Register (CR50)**

Read/Write Address: 3?5H, Index 50H

Power-On Default: 00H

7	6	5	4	3	2	1	0
GE-SCR-W		PXL-LNGH		R	R	R	GESW
1 0		1 0					2

Bit 0 Extension bit 2 of the screen width definition. See bits 7-6 below.

Bits 3-1 Reserved

Bits 5-4 PXL-LNGH - Pixel Length Select (2D/3D)

- 00 = 1 byte (Default). This corresponds to a pixel length of 4 or 8 bits/pixel in MM850C\_2.
- 01 = 2 bytes. 16 bits/pixel
- 10 = Reserved
- 11 = 4 bytes. 32 bits/pixel

These bits select the pixel length for Enhanced mode command execution through either the 2D or 3D Engines.

Bits 7-6 GE-SCR-W - 2D Graphics Engine Command Screen Pixel Width (2D only)

Bit 0 of this register is the most significant bit of this definition.

- 000 = 1024 (or 2048 if bit 1 of CR31 =1) (Default)
- 001 = 640
- 010 = 800 (or 1600x1200x4 if bit 2 of MM850C\_2 = 0)
- 011 = 1280
- 100 = 1152
- 101 = Reserved
- 110 = 1600
- 111 = Use Global Bitmap Descriptor

**Extended System Control 2 Register (CR51)**

Read/Write Address: 3?5H, Index 51H

Power-On Default: 00H

7	6	5	4	3	2	1	0
ERL	R	LSW9-8		R	R	R	R

Bits 5-0 Reserved

Bits 5-4 LSW9-8 - Logical Screen Width Bits 9-8

These are two extension bits of the Offset register (CR13).

Bits 6 Reserved

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Extended CRTC Registers

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Bit 7      ERL - Enable Register Load  
0 = No effect  
1 = Enable function of CR66\_4 and CR66\_5 (load certain Streams Processor registers on VSYNC)

This bit is automatically cleared to 0 after being set.

---

**Extended BIOS Flag 1 Register (CR52)**

Read/Write                      Address: 3?5H, Index 52H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT BIOS FLAG 1							

Bits 7-0      EXT BIOS FLAG 1

See the S3 video BIOS documentation for the coding of this register.

---

**Extended Memory Control 1 Register (CR53)**

Read/Write                      Address: 3?5H, Index 53H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
VGA MEM	SWP NBL	MMIO WIN	OME	R	R	R	R

Bit 3-0      Reserved

Bit 4      OME Old MMIO Enable  
0 = Disable old MMIO  
1 = Old MMIO enabled

Old MMIO is used only for S3 testing. PCI04\_1, SR9\_7 and bits 5 and 7 of this register also control MMIO accesses. Only new MMIO (enabled by default) should be used for software written for Savage4.

Bit 5      MMIO WIN - Old MMIO Window  
0 = Old MMIO window enabled at A8000H - AFFFFH. A0000H - A7FFF available for image transfers  
1 = Old MMIO window enabled at B8000H - BFFFFH. A0000H - B7FFFH are not used (no image transfer area)

Bit 4 of this register must be programmed to 1 for this bit to be effective.

Bit 6      SWP NBL - Swap Nibbles  
0 = No nibble swap  
1 = Swap nibbles in each byte of a linear memory address read or write operation

Bit 7      VGA MEM - VGA Memory Access Disable  
0 = Enable memory access to A0000-BFFFF address range  
1 = Disable memory access to A0000-BFFFF address range

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Extended CRTC Registers

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**Extended RAMDAC Control Register (CR55)**

Read/Write Address: 3?5H, Index 55H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	HCS	R	R	R	R

Bits 3-0 Reserved

Bit 4 HCS - Hardware Cursor MS/X11 Mode Select  
0 = MS Windows mode (Default)  
1 = X11 Window mode

This bit select the type of decoding used for the 64x64x2 storage array of the hardware graphics cursor.

Bits 7-5 Reserved

---

**External Sync Control 1 Register (CR56)**

Read/Write Address: 3?5H, Index 56H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	TOV	TOH	R

Bit 0 Reserved

Bit 1 TOH - Tri-state off HSYNC  
0 = HSYNC output buffer on  
1 = HSYNC output buffer in hi-Z state

Bit 2 TOV - Tri-state off VSYNC  
0 = VSYNC output buffer on  
1 = VSYNC output buffer in hi-Z state

Bits 7-3 Reserved

---

**Linear Address Window Control Register (CR58)**

Read/Write Address: 3?5H, Index 58H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	ELA	CBO	R	WIN SIZE	

Bits 1-0 WIN SIZE - Linear Addressing Window Size  
00 = Reserved  
01 = Reserved  
10 = Reserved  
11 = 32 MBytes

Bit 2 Reserved

Bit 3 CBO - CPU Base Address Overflow

This is bit 22 of the CPU base address. See CR6A. This function is moved to CR92\_5 for Rev. B and this bit is reserved

Bit 4 ELA - Enable Linear Addressing  
0 = Disable linear addressing  
1 = Enable linear addressing

Bits 7-5 Reserved



---

**Linear Address Window Position Register (CR59) (Mapping 1, CRB0\_7 = 0) (Rev. A)**

Read/Write                      Address: 3?5H, Index 59H  
Power-On Default: 70H

7	6	5	4	3	2	1	0
LA WINDOW POSITION							

Bits 7-0      LA WINDOW POSITION

Value = Bits 31-24 of linear addressing window position

These bits are common with bits 31-24 of the PCI base address 1 for address mapping 1. A write to either register updates both. However, the base address is normally programmed by the system BIOS and should never be changed via this register except for test purposes. Note that only 16 MBytes can be accessed at this base address when using address mapping 1.

---

**Linear Address Window Position Register (CR59) (Mapping 1, CRB0\_7 = 0) (Rev. B)**

Read/Write                      Address: 3?5H, Index 59H  
Power-On Default: 70H

7	6	5	4	3	2	1	0
LA WINDOW POSITION							R

Bits 7-0      LA WINDOW POSITION

Value = Bits 31-25 of linear addressing window position

These bits are common with bits 31-25 of the PCI base address 1 for address mapping 1. A write to either register updates both. However, the base address is normally programmed by the system BIOS and should never be changed via this register except for test purposes. Note that only 16 MBytes can be accessed at this base address when using address mapping 1.

---

**Linear Address Window Position Register (CR59) (Mapping 0, CRB0\_7 = 1)**

Read/Write                      Address: 3?5H, Index 59H  
Power-On Default: 70H

7	6	5	4	3	2	1	0
LA WINDOW POSITION					R	R	R

Bits 2-0      Reserved

Bits 7-3      LA WINDOW POSITION

Value = Bits 31-27 of linear addressing window position

These bits are common with bits 31-27 of the PCI base address 1 for address mapping 0. A write to either register updates both. However, the base address is normally programmed by the system BIOS and should never be changed via this register except for test purposes.

Extended CRTC Registers

**Extended Horizontal Overflow 2 Register (CR5B)**

Read/Write Address: 3?5H, Index 5BH

Power-On Default: 00H

7	6	5	4	3	2	1	0
EHS6-5		EHB7-6		SFF10-9		IRP9-8	

- Bits 1-0 IRP9-8 - Interlace Restart Position (CR3C) Bits 9-8
- Bits 3-2 SFF10-9 - Start FIFO Fetch (CR3B) Bits 10-9
- Bits 5-4 EHB7-6 - End Horizontal Blank (CR3\_4-0, CR5\_7) Bits 7-6
- This is only valid when SR5D\_7 = 1.
- Bits 7-6 EHS6-5 - End Horizontal Blank (CR5\_4-0) Bits 6-5
- This is only valid when SR5D\_7 = 1.

**General Output Port Register (CR5C)**

Read/Write Address: 3?5H, Index 5CH

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	GOP0

- Bit 0 GOP0
- The state of this bit is reflected on the GOP0 pin.
- Bits 7-1 Reserved

**Extended Horizontal Overflow 0 Register (CR5D)**

Read/Write Address: 3?5H, Index 5DH

Power-On Default: 00H

7	6	5	4	3	2	1	0
NMS	SFF 8	HSP	SHS 8	HBP	SHB 8	HDE 8	HT 8

- Bit 0 HT 8 - Horizontal Total (CR0) Bit 8
- Bit 1 HDE 8 - Horizontal Display End (CR1) Bit 8
- Bit 2 SHB 8 - Start Horizontal Blank (CR2) Bit 8
- Bit 3 HBP - Horizontal Blank Period
- 0 = Horizontal blank period is equal to or less than 64 character clocks (256 character clocks if CR5D\_7 = 1)
- 1 = Horizontal blank period is greater than 64 character clocks (256 character clocks if CR5D\_7 = 1)
- See CR3\_4-0.
- Bit 4 SHS 8 - Start Horizontal Sync Position (CR4) Bit 8
- Bit 5 HSP - Horizontal Sync Period
- 0 = Horizontal sync period is equal to or less than 32 character clocks (128 character clocks if CR5D\_7 = 1)
- 1 = Horizontal sync period is greater than 32 character clocks (128 character clocks if CR5D\_7 = 1)
- See CR5\_4-0.

Extended CRTC Registers

- Bit 6 SFF 8 - Start FIFO Fetch (CR3B) Bit 8
- Bit 7 NMS - New Mode Support  
0 = All modes except 1280x1024x24  
1 = 1280x1024x24 mode

When this bit is set, the end horizontal blank (CR3\_4-0, CR5\_7) and end horizontal sync (CR5\_4-0) parameters have new definitions and CR5B\_7-4 must be programmed.

**Extended Vertical Overflow Register (CR5E)**

Read/Write Address: 3?5H, Index 5EH  
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	LCM 10	R	VRS 10	R	SVB 10	VDE 10	VT 10

- Bit 0 VT 10 - Vertical Total (CR6) Bit 10
- Bit 1 VDE 10 - Vertical Display End (CR12) Bit 10
- Bit 2 SVB 10 - Start Vertical Blank (CR15) Bit 10
- Bit 3 Reserved
- Bit 4 VRS 10 - Vertical Retrace Start (CR10) Bit 10
- Bit 5 Reserved
- Bit 6 LCM 10 - Line Compare Position (CR18) Bit 10
- Bit 7 Reserved

**Extended Horizontal Overflow 1 Register (CR5F)**

Read/Write Address: 3?5H, Index 5FH  
Power-On Default: 00H

7	6	5	4	3	2	1	0
SHS10-9		SHB10-9		HDE10-9		HT10-9	

- Bits 1-0 HT10-9 - Horizontal Total (CR0) Bits 10-9
- Bits 3-2 HDE10-9 - Horizontal Display End (CR1) Bits 10-9
- Bits 5-4 SHB10-9 - Start Horizontal Blank (CR2) Bits 10-9
- Bits 7-6 SHS10-9 - Start Horizontal Sync Position (CR4) Bits 10-9 ]

Extended CRTC Registers

**SDCLK Skew Register (CR60)**

Read/Write Address: 3?5H, Index 60H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	SDCLKX SKEW			

Bits 3-0 SDCLKX SKEW  
 0000 = SDCLKX not skewed  
 0001 = SDCLKX generated 9 units earlier than 0000 setting  
 0010 = SDCLKX generated 8 units earlier than 0000 setting  
 0011 = SDCLKX generated 7 units earlier than 0000 setting  
 0100 = SDCLKX generated 6 units earlier than 0000 setting  
 0101 = SDCLKX generated 5 units earlier than 0000 setting  
 0110 = SDCLKX generated 4 units earlier than 0000 setting  
 0111 = SDCLKX generated 3 units earlier than 0000 setting  
 1000 = SDCLKX generated 2 units earlier than 0000 setting  
 1001 = SDCLKX generated 1 unit earlier than 0000 setting  
 1010 = SDCLKX generated 1 unit later than 0000 setting  
 1011 = SDCLKX generated 2 units later than 0000 setting  
 1100 = SDCLKX generated 3 units later than 0000 setting  
 1101 = SDCLKX generated 4 units later than 0000 setting  
 1110 = SDCLKX generated 5 units later than 0000 setting  
 1111 = SDCLKX generated 6 units later than 0000 setting

SDCLKX = SDCLK1, SDCLK2 and SDCLKOUT

Bits 7-4 Reserved

**Extended Miscellaneous Control Register (CR65)**

Read/Write Address: 3?5H, Index 65H

Power-On Default: 00H

7	6	5	4	3	2	1	0
DLY HDE	R	DLY BLANK	R	R	DH		

Bit 0 DH - See bits 7-6 below.

Bits 2-1 Reserved

Bits 4-3 DLY BLANK - Delay BLANK by DCLK  
 00 = No delay of BLANK  
 01 = Delay BLANK for 1 DCLK  
 10 = Delay BLANK for 2 DCLKs  
 11 = Delay BLANK for 3 DCLKs  
 BLANK is an internal signal. This function will not normally be used.

Bit 5 Reserved

Bits 0, 7-6 DLY HDE - Delay Horizontal Display Enable  
 000 = No delay  
 001 = 1 DCLK delay  
 010 = 2 DCLK delay  
 011 = 3 DCLK delay  
 100 = 4 DCLK delay  
 101 = 5 DCLK delay  
 110 = 6 DCLK delay  
 111 = 7 DCLK delay

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Extended CRTC Registers

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**Extended Miscellaneous Control 1 Register (CR66)**


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Read/Write Address: 3?5H, Index 66H

Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI RET	R	RLC	R	PCI DIS	R	SW RST	EN 2D/3D

Bit 0 EN 2D/3D - Enable 2D/3D Engine Operation  
0 = Disable 2D/3D Engine operation  
1 = Enable 2D/3D Engine operation

This bit must only be programmed during screen off (SR1\_5 = 1) or during the vertical retrace period. Setting SR1\_5 to 1 may take up to 3 HSYNCs to take effect. This bit is ORed with MM850C\_0. This bit must be set to 1 for mastered image transfers.

Bit 1 SW RST - Software Reset  
0 = No function  
1 = Software reset of the 2D Graphics Engine

Setting this bit has the same effect as MM8504\_15-14 (write) = 10b.

Bit 2 Reserved

Bit 3 PCI DIS - PCI Disconnect Enable  
0 = PCI disconnects disabled  
1 = PCI disconnects enabled

This bit must be set to 1 by the video BIOS.

Bit 4 PLC - Primary Stream Register Loading Control  
0 = Load certain working primary stream registers when VSYNC active  
1 = Load certain working primary streams registers when CR51\_7 = 1 (or PageFlip command issued) and VSYNC active

This bit applies to those primary stream registers that are programmed to shadow registers. These are MM81C0 and MM81C4.

Bit 5 SLC - Secondary Stream Register Loading Control  
0 = Load working secondary stream registers when VSYNC active  
1 = Load working secondary stream registers when CR51\_7 = 1 and VSYNC active

This bit applies to those secondary stream registers that are programmed to a shadow register and the new values do not take effect until the next VSYNC. These are MM8190, MM8198, MM81A0, MM81D0, MM81D4, MM81D8, MM81E0, MM81E4 and MM81E8, MM8304, MM8308.

Bit 6 Reserved

Bit 7 PCI RET - PCI Retry Enable  
0 = PCI bus retry disabled  
1 = PCI bus retry enabled

This bit does not apply to AGP operation.

**Extended Miscellaneous Control 2 Register (CR67)**

Read/Write Address: 3?5H, Index 67H

Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR MODE				STREAMS MODE		R	VCLK PHS

Bit 0 VCLK PHS - VCLK Phase With Respect to DCLK  
0 = VCLK is 180° out of phase with DCLK (inverted)  
1 = VCLK is in phase with DCLK

Pixels are clocked out of the RAMDAC at the VCLK rate.

Bit 1 Reserved

Bits 3-2 STREAMS MODE  
00 = Streams Processor disabled  
01 = Primary Stream data from graphics controller with secondary stream overlay  
10 = Reserved  
11 = Full Streams Processor operation (primary and secondary streams from all supported sources)

The Streams Processor should only be enabled or disabled during the VSYNC period. The 01 setting is required for automatic centering and expansion of the flat panel display with the Streams Processor enabled. See CR90\_3 and CR90\_6.

Bits 7-4 COLOR MODE - RAMDAC Color Mode  
0000 = 8-bit color  
0001 = 8-bit color, clock doubled  
0010 = 15-bit color (X.5.5.5)  
0011 = 15-bit color, (X.5.5.5) clock doubled  
0100 = 16-bit color (5.6.5)  
0101 = 16-bit color (5.6.5) clock doubled  
1101 = 32-bit color (X.8.8.8)

All other mode values are reserved. This field is only valid when Streams Processor operation is disabled (CR67\_3-2 = 00b). With the Streams Processor enabled, the color mode is defined by MM8180\_26-24. Clock doubled modes require that SR18\_7 = 1 and SR15\_4 = 1.

**Memory Control 1 Register (CR68)**

Read/Write Address: 3?5H, Index 68H

Power-On Default: 00H

These bits can be accessed only after A5H is written to CR39.

7	6	5	4	3	2	1	0
MTS		TRP		TRAS	TDPL	TRC	

Bits 1-0 TRC - SGRAM Auto Refresh to New Command  
00 = 7 MCLKs  
01 = 8 MCLKs  
10 = 9 MCLKs  
11 = 10 MCLKs

This is the time from a CAS before RAS refresh cycle to the next refresh cycle or activate command.

Bit 2 TDPL - SGRAM Last Data In to Row Precharge Delay (Write Cycle)  
0 = 1 MCLK  
1 = 2 MCLKs

Extended CRTC Registers

- Bit 3      TRAS - Minimum -SDRAS Low Timing Select  
 0 = 6 MCLKs  
 1 = 7 MCLKs

This value assumes a single command (e.g., read) is executed. The time will extend one clock for each additional command.
- Bits 5-4    TRP - -SDRAS Precharge Time  
 00 = Reserved  
 01 = Reserved  
 10 = 2 MCLKs  
 11 = 3 MCLKs

This is the time from a precharge command to a refresh cycle (if required) or the next activate command.
- Bits 7-6    MTS - Memory Type Select  
 00 = 2Mx32 (SDRAM) (including 32MB, 4 bank , CR36\_7-5 = 111, CR92\_6 = 1 – Rev B)  
 01 = 1Mx16 (SDRAM) (up to 16MB, CR92\_6 = 0) or [2Mx32 4 bank SDRAM (8 MB, CR36\_7-5 = 001, CR92\_6 = 1, Rev B)]  
 01 = 2MX32 (4 Bank SDRAM) (16MB, CR92\_6 = 1)  
 01 = 4MX16 (4 Bank SDRAM) (32MB)  
 10 = 512Kx32 (SGRAM)  
 11 = 256Kx32 (SGRAM)

**Extended System Control 3 Register (CR69)**

Read/Write                      Address: 3?5H, Index 69H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
PS      DISPLAY START ADDRESS							

- Bits 6-0      DISPLAY START ADDRESS

Value = the upper 7 bits (22-16) of the display start address

This allows addressing of up to 32 MBytes of display memory.
- Bit 7      PS - Primary Stream Definition  
 0 = Standard VGA registers are used to control the primary stream  
 1 = Memory mapped registers MM81C0 and MM81C4 are used to control the primary stream.

**Extended System Control 4 Register (CR6A)**

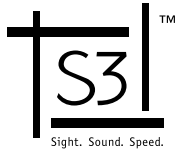
Read/Write                      Address: 3?5H, Index 6AH  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
CPU BASE ADDRESS							

- Bits 7-0      CPU BASE ADDRESS

Value = Bits 21-14 of the CPU base address

Bit 22 is CR58\_3. This allows accessing of up to 32 MBytes of display memory via 64K pages. Bit 0 of CR31 must be set to 1 to enable this field. If linear addressing is enabled and a 64 KByte window is specified, these bits specify the 64K page to be accessed at A0000H.



Extended CRTC Registers

**Extended BIOS Flag 3 Register (CR6B)**

Read/Write Address: 3?5H, Index 6BH

Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-3							

Bits 7-0 EXT-BIOS-FLAG-REGISTER-3  
This register is reserved for use by the S3 BIOS.

**Extended BIOS Flag 4 Register (CR6C)**

Read/Write Address: 3?5H, Index 6CH

Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-4							

Bits 7-0 EXT-BIOS-FLAG-REGISTER-4  
This register is reserved for use by the S3 BIOS.

**Extended BIOS Flag 5 Register (CR6D)**

Read/Write Address: 3?5H, Index 6DH

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**DAC Signature Test Data Register (CR6E)**

Read/Write Address: 3?5H, Index 6EH

Power-On Default: 00H

7	6	5	4	3	2	1	0
DAC SIGNATURE TEST DATA							

Bits 7-0 DAC SIGNATURE TEST DATA



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Extended CRTC Registers

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**Memory Control 2 Register (CR6F)**

Read/Write Address: 3?5H, Index 6FH

Power-On Default: FEH

These bits can be accessed only after A5H is written to CR39.

7	6	5	4	3	2	1	0
R	CAS LATENCY	R	TRRD	R	R	R	SR

Bit 0 SR - Software Reset Enable  
0 = Software resets disabled (default)  
1 = Software resets enabled

This bit controls the resets in CR3F. It should be set only if CR3F is to be programmed, and should be immediately cleared to 0 after programming CR3F.

Bits 2-1 Reserved

Bit 3 TRRD - SGRAM Time Interval Select for Consecutive Bank Activation  
0 = 2 MCLKs  
1 = 3 MCLKs

Bit 4 Reserved

Bits 6-5 SGRAM CAS Latency  
00 = 4 MCLKs  
01 = 4 MCLKs  
10 = 2 MCLKs  
11 = 3 MCLKs

Bit 7 Reserved

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**AGP Control Register (CR70)**

Read/Write Address: 3?5H, Index 70H

Power-On Default: 00H

7	6	5	4	3	2	1	0
SB	R	NW	ACS	SSS	ASM	AP	ACS

Bit 0 ACS - AGP Command Suspend  
0 = Normal operation or resume from suspend  
1 = Suspend sending commands to system logic

The suspend mode is selected via bit 2 of this register.

Bit 1 AP - AGP Priority  
0 = Always send low priority commands  
1 = Always send high priority commands

Bit 2 ASM - AGP Suspend Mode  
0 = Pause sending of commands to system logic. Resume from previous operating state when bit 0 of this register is cleared to 0.  
1 = Reset. All current commands discarded. Resume from initial idle state when bit 0 of this register is cleared to 0.

Bit 3 SSS - Stop Sideband Strobe  
0 = SB\_STB signal is kept running when bit 0 of this register is set to 1  
1 = SB\_STB signal is stopped when bit 0 of this register is set to 1

Bit 4 ACS - AGP Command Split  
0 = Normal operation  
1 = Split AGP reads into 32-byte bursts

Extended CRTC Registers

- Bit 5      NW - AGP No Wait  
0 = 1 SCLK delay between -GNT assertion and -PIPE assertion  
1 = No delay between -GNT assertion and -PIPE assertion
- Bit 6      Reserved
- Bit 7      SB - AGP Sideband Addressing Capability  
0 = Set PCI84\_9 to 0 (sideband addressing not supported)  
1 = Set PCI84\_0 to 1 (sideband addressing supported)

**Primary Stream Timeout Register (CR71)**

Read/Write                      Address: 3?5H, Index 71H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
PRIMARY STREAM TIMEOUT COUNT							

Bits 7-0      PRIMARY STREAM TIMEOUT COUNT  
  
Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed  
  
If CR88\_2 = 1, the count is in MCLKs.

**TV Timeout Register (CR72)**

Read/Write                      Address: 3?5H, Index 72H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
TV TIMEOUT COUNT							

Bits 7-0      TV TIMEOUT COUNT  
  
Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed  
  
If CR88\_2 = 1, the count is in MCLKs.

**Secondary Stream Timeout Register (CR73)**

Read/Write                      Address: 3?5H, Index 73H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
SECONDARY STREAM TIMEOUT COUNT							

Bits 7-0      SECONDARY STREAM TIMEOUT COUNT  
  
Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed  
  
If CR88\_2 = 1, the count is in MCLKs.

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Extended CRTC Registers

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**Master Control Unit Timeout Register (CR74)**

Read/Write Address: 3?5H, Index 74H

Power-On Default: 00H

7	6	5	4	3	2	1	0
MASTER CONTROL UNIT TIMEOUT COUNT							

Bits 7-0 MASTER CONTROL UNIT TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

---

**Command Buffer Timeout Register (CR75)**

Read/Write Address: 3?5H, Index 75H

Power-On Default: 00H

7	6	5	4	3	2	1	0
COMMAND BUFFER TIMEOUT COUNT							

Bits 7-0 COMMAND BUFFER TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

---

**LPB Timeout Register (CR76)**

Read/Write Address: 3?5H, Index 76H

Power-On Default: 00H

7	6	5	4	3	2	1	0
LPB TIMEOUT COUNT							

Bits 7-0 LPB TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

---

**Motion Compensation Timeout Register (CR77)**

Read/Write Address: 3?5H, Index 77H

Power-On Default: 00H

7	6	5	4	3	2	1	0
MOTION COMPENSATION TIMEOUT COUNT							

Bits 7-0 MOTION COMPENSATION TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

---

**CPU Timeout Register (CR78)**

Read/Write                      Address: 3?5H, Index 78H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
CPU TIMEOUT COUNT							

Bits 7-0            CPU TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

---

**2D Graphics Engine Timeout Register (CR79)**

Read/Write                      Address: 3?5H, Index 79H  
Power-On Default: 00H

7	6	5	4	3	2	1	0
2D GRAPHICS ENGINE TIMEOUT COUNT							

Bits 7-0            2D GRAPHICS ENGINE TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

---

**3D Z Read Buffer Timeout Register (CR7A)**

Read/Write                      Address: 3?5H, Index 7AH  
Power-On Default: 00H

7	6	5	4	3	2	1	0
3D Z READ BUFFER TIMEOUT COUNT							

Bits 7-0            3D ENGINE Z READ BUFFER TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

**3D Z Write Buffer Timeout Register (CR7B)**

Read/Write Address: 3?5H, Index 7BH

Power-On Default: 00H

7	6	5	4	3	2	1	0
3D ENGINE Z WRITE BUFFER TIMEOUT COUNT							

Bits 7-0 3D ENGINE Z WRITE BUFFER TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed  
If CR88\_2 = 1, the count is in MCLKs.

**3D Destination Write Timeout Register (CR7C)**

Read/Write Address: 3?5H, Index 7CH

Power-On Default: 00H

7	6	5	4	3	2	1	0
3D DESTINATION WRITE TIMEOUT COUNT							

Bits 7-0 3D DESTINATION WRITE TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

**3D Destination Read Timeout Register (CR7D)**

Read/Write Address: 3?5H, Index 7DH

Power-On Default: 00H

7	6	5	4	3	2	1	0
3D DESTINATION READ TIMEOUT COUNT							

Bits 7-0 3D DESTINATION READ TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

---

**3D Texture Buffer Timeout Register (CR7E)**

Read/Write Address: 3?5H, Index 7EH

Power-On Default: 00H

7	6	5	4	3	2	1	0
3D TEXTURE BUFFER TIMEOUT COUNT							

Bits 7-0 3D TEXTURE BUFFER TIMEOUT COUNT

Value = # of QWords transferred to/from the frame buffer before the memory bus grant is removed

If CR88\_2 = 1, the count is in MCLKs.

---

**Drive Current Control Register (CR80)**

Read/Write Address: 3?5H, Index 80H

Power-On Default: 00H

7	6	5	4	3	2	1	0
SDD	MCD	MAD	PDD	R	SBD	PCD	

Bits 1-0 PCD - PCI/AGP Drive Current (3.3V VDDq)  
00 = 24 mA (default for PCI bus operation (CR37\_6 = 0))  
01 = 16 mA (default for AGP bus operation (CR37\_6 = 1))  
10 = 8 mA  
11 = 4 mA

This bit applies to AD[31:0], -C/BE[3:0], PAR, -FRAME, -IRDY, -TRDY, -STOP, -DEVSEL, -REQ, -PIPE, AD\_STB[1:0], -AD\_STB[1:0] and -RBF. Bit 0 is the same bit as CR37\_6 and its value at reset depends on strapping of the ROMA3 pin.

Bit 2 SB - SBA[7:0], SB\_STB, -SB\_STR Drive Current  
0 = 8 mA  
1 = 16 mA

Bit 3 Reserved

Bit 4 PDD - PD[63:0] Drive Current  
0 = 16 mA  
1 = 8 mA

Bit 5 MAD - MA[10:0] Drive Current  
0 = 16 mA  
1 = 8 mA

Bit 6 MCD - Memory Control Drive Current  
0 = 16 mA  
1 = 8 mA

This bit applies to -RAS, -CAS, -WE, -DSF, CKE, -CS[1:0] AND DQM[7:0].

Bit 7 SDD - SDCLK[1:2] Drive Current  
0 = 24 mA  
1 = 16 mA

**PCI Subsystem Vendor ID Shadow Low Register (CR81)**

Read/Write Address: 3?5H, Index 81H

Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI SUBSYSTEM VENDOR ID LOW BYTE							

Bits 7-0 PCI SUBSYSTEM VENDOR ID LOW BYTE)

This register shadows the byte at PCI configuration space index 2CH.

**PCI Subsystem Vendor ID Shadow High Register (CR82)**

Read/Write Address: 3?5H, Index 82H

Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI SUBSYSTEM VENDOR ID HIGH BYTE							

Bits 7-0 PCI SUBSYSTEM VENDOR ID HIGH BYTE)

This register shadows the byte at PCI configuration space index 2DH.

**PCI Subsystem ID Shadow Low Register (CR83)**

Read/Write Address: 3?5H, Index 83H

Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI SUBSYSTEM ID LOW BYTE							

Bits 7-0 PCI SUBSYSTEM ID LOW BYTE)

This register shadows the byte at PCI configuration space index 2EH.

**PCI Subsystem ID Shadow High Register (CR84)**

Read/Write Address: 3?5H, Index 84H

Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI SUBSYSTEM ID HIGH BYTE							

Bits 7-0 PCI SUBSYSTEM ID HIGH BYTE)

This register shadows the byte at PCI configuration space index 2FH.

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Extended CRTC Registers

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**FIFO Fetch Delay Register (CR85)**

Read/Write Address: 3?5H, Index 85H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	FDE	R	FIFO DRAIN DELAY		

Bits 2-0 FIFO DRAIN DELAY

Value = number of character clocks to delay draining of the display FIFO with respect to the request for FIFO filling.

A high value may be required in some cases to prevent draining of data from the display (primary/secondary stream) FIFO before valid data has been fetched from memory into the FIFO. The optimum value must be determined empirically. A starting value of 010b is recommended. In general, the smallest value that works should be used. Bit 4 of this register must be set to 1 for these bits to be effective.

Bit 3 Reserved

Bit 4 FFT - FIFO Fetch Timing

0 = Fetch primary and secondary stream data from memory at the end of the horizontal blanking region

1 = Fetch primary and secondary stream data from memory in the middle of the horizontal blanking region

This bit should be set to 1 for all accelerated modes.

Bits 7-5 Reserved

**DAC Power Up Register (CR86)**

Read/Write Address: 3?5H, Index 86H

Power-On Default: 00H

7	6	5	4	3	2	1	0
DPSD	DAC POWER UP TIME						

Bits 6-0 DAC POWER UP TIME

value = number of character clocks from the start of blanking at which the internal DACs are powered up

This value must be at least 1 less than the End Horizontal Blank value programmed in CR5D\_3, CR5\_7 and CR3\_4-0. A value of 1 less starts DAC power up 1 character clock before the end of blanking. A value of 2 less starts DAC power up 2 character clocks before the end of blanking, etc. When the DACs power up, there is a voltage spike that affects the RGB outputs if they are active. Powering up the DACs earlier reduces the power savings but also reduces the chance that the power up voltage spike will affect the active display.

Bit 7 DPSD - DAC Power Saving Disable

0 = RAMDAC power saving enabled (DAC turned off at BLANK start and on at position programmed in bits 6-0 of this register)

1 = RAMDAC power saving disabled (RAMDAC never powered down)

**SGRAM Control 0 Register (CR87)**

Read/Write Address: 3?5H, Index 87H

Power-On Default: 00H

7	6	5	4	3	2	1	0
LWP	R	REFRESH	R	R	R	R	BWC

Bit 0 BWC - Block Write Cycles

0 = 2-cycle block write

1 = 1 cycle block write



**Extended CRTC Registers**

- Bits 3-1      Reserved for S3 Testing
  - Bits 5-4      REFRESH
    - 00 = Select 100 MHz MCLK to count refresh counter
    - 01 = Select 125 MHz MCLK to count refresh counter
    - 10 = Select 143 MHz MCLK to count refresh counter
    - 11 = Reserved for S3 testing
  - Bit 6          Reserved
  - Bit 7          LWP - LPB Write Priority
    - 0 = Normal LPB memory write access priority
    - 1 = High LPB memory write access priority
- Setting this bit may prevent tearing of the live video display.

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**SGRAM Control 1 Register (CR88)**

Read/Write                      Address: 3?5H, Index 88H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
R	DR	MS	DBW	R	TOC	BPL	RCD

- Bit 0          RCD - SGRAM TRCD Parameter
  - 0 = 3 MCLKs
  - 1 = 2 MCLKs
- Bit 1          BPL - SGRAM TBPL Parameter
  - 0 = 3 MCLKs
  - 1 = 2 MCLKs
- Bit 2          TOC - Timeout Counter
  - 0 = Timeout count is in QWords
  - 1 = Timeout count is in MCLKs

This bit applies to the timeout counters in CR71-CR7E.
- Bit 3          Reserved
- Bit 4          DBW - Disable Block Write (2D Engine Only)
  - 0 = Block write enabled
  - 1 = Block write disabled

Block write is used for solid rectangle fills. The drawing direction must be x and y positive (right to left, top to bottom) and the stride must be a multiple of 64.
- Bit 5          MS - SGRAM Mode Set
  - This bit is programmed to 1 to generate a mode programming cycle. This bit is automatically cleared to 0 after the programming cycle.
- Bit 6          DR - Disable SGRAM Refresh
  - 0 = Refresh enabled
  - 1 = Refresh disabled
- Bit 7          Reserved

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Extended CRTC Registers

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**Primary Stream FIFO Fetch Control 1 Register (CR90)**

Read/Write Address: 3?5H, Index 90H

Power-On Default: 00H

7	6	5	4	3	2	1	0
EL1	FP1	SFRD		FP2	L1 10-8		

- Bits 2-0 L1 10-8 - Primary Stream L1 Parameter (Bits 10-8)  
These are bits 10-8 of the primary stream L1 parameter. See the description of the primary stream L1 parameter in the description for CR91.
- Bit 3 FP1 - Flat Panel Output Control Bit 1  
0 = Streams Processor off or full on (CR67\_3-2 = 00 or 11) or 8bpp with Streams Processor (CR67\_3-2 = 01)  
1 = 15/16 or 32 bpp primary stream output with automatic centering and expansion (CR67\_3-2 = 01)
- Bit 6 of this register must also be set to 1 for this bit to be effective.
- Bits 5-4 SFRD - Streams FIFO Reset Delay  
00 = No delay  
01 = 1 character clock delay  
10 = 2 character clocks delay  
11 = 3 character clocks delay
- Bit 6 FP2 - Flat Panel Output Control Bit 2  
0 = Streams Processor off or full on (CR67\_3-2 = 00 or 11)  
1 = Enable primary stream output with automatic centering and expansion (all color depths) (CR67\_3-2 = 01)
- Bit 7 EL1 - Enable L1 Parameter  
0 = Primary stream display fetch length control (L1 parameter) disabled  
1 = Primary stream display fetch length control (L1 parameter) enabled

---

**Primary Stream FIFO Fetch Control 2 Register (CR91)**

Read/Write Address: 3?5H, Index 91H

Power-On Default: 00H

These are the lower 8 bits of an 11-bit value used to optimize performance. The upper three bits are bits 2-0 of CR90.

7	6	5	4	3	2	1	0
L1 7-0							

- Bits 7-0 L1 7-0 - Primary Stream L1 Parameter (Bits 7-0)
- 11-bit Value = [(number of bytes of displayed pixels per scan line) ÷ 8] - 1. This register contains the least significant 8 bits of this value.

**Secondary Stream FIFO Fetch Control 1 Register (CR92)**

Read/Write Address: 3?5H, Index 92H

Power-On Default: 00H

When writing the L parameter bits in this register, ensure that bit 6 is not changed.

7	6	5	4	3	2	1	0
EL2	4B			R		L2 10-8	

- Bits 2-0 L2 10-8 - Secondary Stream L2 Parameter (Bits 10-8)  
These are bits 10-8 of the secondary stream L2 parameter. See the description of the primary stream L2 parameter in the description for CR93.
- Bit 3 Reserved
- Bit 4 LT – Savage4 LT Indicator (read only)(Rev. B)  
0 = Savage4 LT chip  
1 = Other Savage4 family chip
- Bit 5 CA – CPU Base Address Overflow Bit (Rev. B)  
  
Value = CPU base address bit 22  
  
This bit is moved from CR58\_3 for Rev. A
- Bits 6 4B - 4 Bank Support  
0 = Setting for CR68\_7-6 = 01 with 1MX16 SDRAM  
1 = Setting for CR68\_7-6 = 01 with 16 MBytes of 2MX32 4-Bank SDRAM
- Bit 7 EL2 - Enable S L2 Parameter  
0 = Secondary stream display fetch length control (L2 parameter) disabled  
1 = Secondary stream display fetch length control (L2 parameter) enabled

**Secondary Stream FIFO Fetch Control 2 Register (CR93)**

Read/Write Address: 3?5H, Index 93H

Power-On Default: 00H

These are the lower 8 bits of an 11-bit value used to optimize performance. The upper three bits are bits 2-0 of CR92.

7	6	5	4	3	2	1	0
L2 7-0							

- Bits 7-0 L2 7-0 - Secondary Stream L2 Parameter (Bits 7-0)  
  
11-bit Value = [(number of bytes of displayed pixels per scan line) ÷ 8] - 1. This register contains the least significant 8 bits of this value.

---

Extended CRTC Registers

---



---

**Serial Port 1 Register (CRA0)**

Read/Write Address: 3?5H, Index A0H

Power-On Default: 00H

Bits 4-0 of this register can also be accessed via MMFF20\_4-0. This register is normally used for I<sup>2</sup>C communications

7	6	5	4	3	2	1	0
R	R	R	SPE	SDR	SCR	SDW	SCW

- Bit 0 SCW - Serial Clock Write  
0 = SPCLK1 is driven low  
1 = SPCLK1 is tri-stated  
SPCLK1 carries the I2C clock. When the SPCLK pin is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 2 of this register.
- Bit 1 SDW - Serial Data Write  
0 = SPD1 pin is driven low  
1 = SPD1 pin is tri-stated  
SPD1 carries the I2C data. When the SPD1 pin is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 3 of this register.
- Bit 2 SCR - Serial Clock Read (Read Only)  
0 = SPCLK1 is low  
1 = SPCLK1 is tri-stated (no device is driving this line)
- Bit 3 SDR - Serial Data Read (Read Only)  
0 = SPD1 pin is low  
1 = SPD1 pin is tri-stated (no device is driving this line)
- Bit 4 SPE - Serial Port 1 Enable  
0 = Use of bits 1-0 of this register disabled  
1 = Use of bits 1-0 of this register enabled
- Bits 7-5 Reserved

---

**Flash ROM Address 0 Register (CRA1)**

Read/Write Address: 3?5H, Index A1H

Power-On Default: 00H

The ROM address is incremented by one for each access to the flash ROM data register (CRA4).

7	6	5	4	3	2	1	0
FLASH ROM ADDRESS 7-0							

- Bits 7-0 FLASH ROM ADDRESS 7-0
- 20-bit Value = Address of byte to be accessed in flash ROM  
Other bits are in CRA2 and CRA3.

---

**Flash ROM Address 1 Register (CRA2)**

Read/Write Address: 3?5H, Index A2H

Power-On Default: 00H

7	6	5	4	3	2	1	0
FLASH ROM ADDRESS 15-8							

Bits 7-0 FLASH ROM ADDRESS 15-8

20-bit Value = Address of byte to be accessed in flash ROM  
Other bits are in CRA1 and CRA3.

---

**Flash ROM Address 2 Register (CRA3)**

Read/Write Address: 3?5H, Index A3H

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	FLASH ROM ADDRESS 19-16			

Bits 3-0 FLASH ROM ADDRESS 19-16

20-bit Value = Address of byte to be accessed in flash ROM

Other bits are in CRA1 and CRA2.

Bits 7-4 Reserved

---

**Flash ROM Data Register (CRA4)**

Read/Write Address: 3?5H, Index A4H

Power-On Default: 00H

The ROM address is programmed via CRA1, CRA2, CRA3.

7	6	5	4	3	2	1	0
FLASH ROM DATA 7-0							

Bits 7-0 FLASH ROM DATA 7-0

Value = Data to be written to flash ROM

---

**Extended BIOS Flag 6 Register (CRA5)**

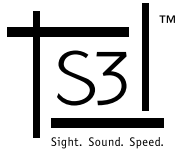
Read/Write Address: 3?5H, Index A5H

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved



Extended CRTC Registers

**Extended BIOS Flag 7 Register (CRA6)**

Read/Write Address: 3?5H, Index A6H

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**Extended BIOS Flag 8 Register (CRA7)**

Read/Write Address: 3?5H, Index A7H

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**Extended BIOS Flag 9 Register (CRA8)**

Read/Write Address: 3?5H, Index A8H

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**Extended BIOS Flag 10 Register (CRA9)**

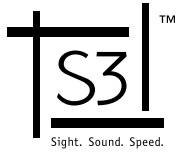
Read/Write Address: 3?5H, Index A9H

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved



Extended CRTC Registers

**Extended BIOS Flag 11 Register (CRAA)**

Read/Write Address: 3?5H, Index AAH

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**Extended BIOS Flag 12 Register (CRAB)**

Read/Write Address: 3?5H, Index ABH

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**Extended BIOS Flag 13 Register (CRAC)**

Read/Write Address: 3?5H, Index ACH

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**Extended BIOS Flag 14 Register (CRAD)**

Read/Write Address: 3?5H, Index ADH

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

Extended CRTC Registers

**Extended BIOS Flag 15 Register (CRAE)**

Read/Write Address: 3?5H, Index AEH

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**Extended BIOS Flag 16 Register (CRAF)**

Read/Write Address: 3?5H, Index AFH

Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7-0 Reserved

**Configuration 3 Register (CRB0)**

Read/Write Address: 3?5H, Index B0H

Power-On Default: Depends on Strapping

If a pin is identified for a bit in this register, the state of that pin is latched at reset. These pins have internal pull-downs and their states are inverted before being latched, so these bits will default to 1 if the corresponding pin is not pulled up externally. If a pin is not associated with a bit, that bit always defaults to 1 at reset. Other configuration bits are found in CR36 and CR37. These bits can be accessed only after A5H is written to CR39.

7	6	5	4	3	2	1	0
AMS	SCS	ST	ETV	FP	ET	R	R

Bit 0 Reserved

Bit 1 Reserved

Bit 2 ET - EPROM Type (ROMA7 pin)  
 0 = Serial SPI EEPROM  
 1 = Parallel EEPROM

Bit 3 FP - Flat Panel Capable (ROMA8 pin)  
 0 = Flat panel connection provided on board  
 1 = Flat panel connection not provided on board

Either a flat panel connection or TV encoder connection can be provided, but not both.

Bit 4 ETV - External TV Encoder Capable (ROMA9 pin)  
 0 = External TV encoder connection provided on board  
 1 = External TV encoder connection not provided on board

Either a flat panel connection or TV encoder connection can be provided, but not both.

Bit 5 ST – Savage4 Type (ROMA10 pin )  
 0 = Savage4 LT or Savage4 GT installed  
 1 = Savage4 Pro or Savage4 Pro-M installed



Extended CRTC Registers

- Bit 6      SCS - SCLK Source  
0 = Use internal clock for PCI signals  
1 = Use external clock input (PCI SCLK) for PCI signals
- Bit 7      AMS - PCI Base Address Map Select (ROMA12 pin)  
0 = Address map 1 (PCI10, 14, 18, 1C, 20, 24)  
1 = Address map 0 (PCI10, 14)

**Serial Port 2 Register (CRB1)**

Read/Write                      Address: 3?5H, Index B1H  
Power-On Default: 00H

This register is normally used for DDC monitor communications.

7	6	5	4	3	2	1	0
R	R	R	SPE	SDR	SCR	SDW	SCW

- Bit 0      SCW - Serial Clock Write  
0 = SPCLK2 is driven low  
1 = SPCLK2 is tri-stated  
  
When the SPCLK2 pin is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 2 of this register.
- Bit 1      SDW - Serial Data Write  
0 = SPD2 pin is driven low  
1 = SPD2 pin is tri-stated  
  
When the SPD2 pin is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 3 of this register.
- Bit 2      SCR - Serial Clock Read (Read Only)  
0 = SPCLK2 is low  
1 = SPCLK2 is tri-stated (no device is driving this line)
- Bit 3      SDR - Serial Data Read (Read Only)  
0 = SPD2 pin is low  
1 = SPD2 pin is tri-stated (no device is driving this line)
- Bit 4      SPE - Serial Port 2 Enable  
0 = Use of bits 1-0 of this register disabled  
1 = Use of bits 1-0 of this register enabled
- Bits 7-5    Reserved

**Serial EEPROM Programming 1 Register (CRB2)**

Read/Write                      Address: 3?5H, Index B2H  
Power-On Default: 00H

This register applies to the first 32K of serial EEPROM.

7	6	5	4	3	2	1	0
SERIAL EEPROM PROGRAMMING/STATUS							

- Bits 7-0      SERIAL EEPROM PROGRAMMING/STATUS  
  
Programming these bits initiates a read or write cycle to the serial EEPROM. The content and protocol are a function of the specific EEPROM used.

---

**Serial EEPROM Programming 2 Register (CRB3)**

Read/Write Address: 3?5H, Index B2H

Power-On Default: 00H

This register applies to the first 32K of serial EEPROM.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	WLC

Bit 0 WLC  
0 = Disable writing to serial EEPROM  
1 = Enable writing to serial EEPROM

Bits 7-1 Reserved

---

**Serial EEPROM Programming 3 Register (CRB4)**

Read/Write Address: 3?5H, Index B4H

Power-On Default: 00H

This register applies to the second 32K of serial EEPROM.

7	6	5	4	3	2	1	0
SERIAL EEPROM PROGRAMMING/STATUS							

Bits 7-0 SERIAL EEPROM PROGRAMMING/STATUS

Programming these bits initiates a read or write cycle to the serial EEPROM. The content and protocol are a function of the specific EEPROM used.

---

**Serial EEPROM Programming 4 Register (CRB5)**

Read/Write Address: 3?5H, Index B5H

Power-On Default: 00H

This register applies to the second 32K of serial EEPROM.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	WLC

Bit 0 WLC  
0 = Disable writing to serial EEPROM  
1 = Enable writing to serial EEPROM

Bits 7-1 Reserved

**Compensation Code Register (CRB6) (Rev. B)**

Write Only                      Address: 3?5H, Index B6H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
NMOS COMP				PMOS COMP			

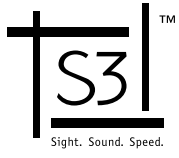
Bits 3-0      PMOS COMP – Compensation Code for PMOS  
                  Value = Compensation code to be used when SR39\_5 = 1  
 Bits 7-4      NMOS COMP – Compensation Code for NMOS  
                  Value = Compensation code to be used when SR39\_5 = 1

**AGP 2x Clock Control Register (CRB7) (Rev. B)**

Read/Write                      Address: 3?5H, Index B7H  
 Power-On Default: 00H

7	6	5	4	3	2	1	0
CE	R	R	R	AGP 2X CLOCK SKEW			

Bits 3-0      AGP 2X CLOCK SKEW  
 0000 = No skew  
 .  
 .  
 .  
 1111 = Maximum Skew  
  
 With bit 7 of this register cleared to 0, this should be initially set to the same value as the 1x clock control in SR1C\_3-0. Then bit 7 of this register is set to 1 to enable 1x to 2x clock phase adjustment. This phase adjustment is then made by adjusting SR1C\_3-0.  
 Bits 6-4      Reserved  
 Bit 7          CE – AGP 2X Clock Skew Control Enable  
 0 = Function of bits 3-0 of this register disabled  
 1 = Function of bits 3-0 of this register enabled



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## Section 6: PCI Register Descriptions

The PCI specification defines a configuration register space. These registers allow device relocation, device independent system address map construction and automatic configurations. The chip provides a subset of these registers, which are described below.

The configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. The chip supports or returns 0 for the first 64 bytes of this space.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined).

---

### Vendor ID (PCI00)

Read Only                      Address: 00H  
 Power-On Default: 5333H

This read-only register identifies the device manufacturer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID															

Bits 15-0      Vendor ID

This is hardwired to 5333H to identify S3 Incorporated.

---

### Device ID (PCI02)

Read Only                      Address: 02H  
 Power-On Default: See Below

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device ID															

Bits 15-0      Device ID

Hardwired to 8A22H

**Command (PCI04)**

See Bit Descriptions Address: 04H

Power-On Default: 0000H

This register controls which types of PCI cycles Savage4 can generate and respond to.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	0	0	0	0	DAC SNP	0	0	BME	MEM	I/O

- Bit 0 I/O - Enable Response to I/O Accesses (Read/Write)  
0 = Response to I/O space accesses is disabled  
1 = Response to I/O space accesses enabled
- Bit 1 MEM - Enable Response to Memory Accesses (Read/Write)  
0 = Response to memory space accesses is disabled  
1 = Response to memory space accesses enabled
- Bit 2 BME - Bus Master Operation Enable (Read/Write)  
0 = Bus master operation disabled  
1 = Bus master operation enabled
- Bit 3 Hardwired to 0 to indicate Savage4 ignores Special Cycles
- Bit 4 Hardwired to 0 to indicate Savage4 cannot initiate the Memory Write and Invalidate command
- Bit 5 DAC SNP - RAMDAC Register Access Snooping (Read/Write)  
0 = Savage4 claims and responds to all RAMDAC register access cycles  
1 = Savage4 performs RAMDAC register writes but does not claim the PCI cycle.  
RAMDAC register read accesses are performed by the Savage4.
- Bit 6 Hardwired to 0 to indicate Savage4 does not detect parity errors
- Bit 7 Hardwired to 0 to indicate Savage4 does not use address/data stepping
- Bit 8 Hardwired to 0 to indicate Savage4 does not generate SERR
- Bit 9 Hardwired to 0 to indicate Savage4 does not generate fast back-to-back master cycles to different targets
- Bits 15-10 Reserved

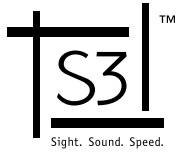
**Status (PCI06)**

Read/Write Address: 06H

Power-On Default: 0230H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	RMA	RTA	STA	DEVSEL	0	0	0	66	CL	R	R	R	R	R

- Bits 3-0 Reserved
- Bit 4 CL - Capabilities List (Read Only)  
  
This bit is hardwired to 1 to indicate a capabilities list is implemented. PCI34\_7-0 point to the first item in the capabilities list.
- Bit 5 66 - 66 MHz Support (Read Only)  
  
This bit is hardwired to 1 to indicate support for 66 MHz operation
- Bit 6 Hardwired to 0 to indicate Savage4 does not support User Definable Features
- Bit 7 Hardwired to 0 to indicate Savage4 does not accept fast back-to-back transactions
- Bit 8 Hardwired to 0 to indicate Savage4 does not detect parity errors.
- Bits 10-9 DEVSEL - Device Select Timing (Read Only)  
01 = Medium DEVSEL timing. (hardwired)



- Bit 11      STA - Signaled Target Abort  
0 = No effect  
1 = PCI slave transaction terminated with target-abort
  
- This bit is reset by software by writing a 1 to this location.
- Bit 12      RTA - Received Target Abort  
0 = No effect  
1 = Bus master transaction terminated with target-abort
  
- This bit is reset by software by writing a 1 to this location.
- Bit 13      RMA - Received Master Abort  
0 = No effect  
1 = Bus master transaction terminated with master-abort
  
- This bit is reset by software by writing a 1 to this location.
- Bit 14      Hardwired to 0 to indicate Savage4 does not assert SERR
- Bit 15      Hardwired to 0 to indicate Savage4 does not check parity

**Class Code (PCI08)**

Read Only                      Address: 08H  
Power-On Default: 030000xxH

This register is hardwired to 030000xxH to specify Savage4 is a VGA-compatible display controller. The xx will change with each revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGRAMMING INTERFACE								REVISION ID							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE CLASS CODE								SUB-CLASS							

**Cache Line Size (PCI0C)**

Read/Write                      Address: 0CH  
Power-On Default: 00H

7	6	5	4	3	2	1	0
CACHE LINE SIZE							

Bits 7-0      Hardwired to 00H because Savage4 does not initiate Master Write and Invalidate commands

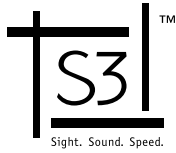
**Latency Timer (PCI0D)**

Read/Write                      Address: 0DH  
Power-On Default: 00H

7	6	5	4	3	2	1	0
BM LATENCY TIMER					0	0	0

Bits 2-0      Reserved = 0

These are the 3 LSB's of the latency timer value, providing 8 clocks granularity.



Bits 7-3 BM LATENCY TIMER - Bus Master Latency Timer

Value = number of PCI clocks the Savage4 can keep its bus master grant without having it removed

These are the 5 MSBs of this value. The three LSBs are 000b. This value is normally programmed by the system BIOS based in part on the requested value in bits 15-8 of 3EH.

**Header Type (PCI0E)**

Read/Write Address: 0EH

Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved

**BIST (PCI0F)**

Read/Write Address: 0FH

Power-On Default: 00H

7	6	5	4	3	2	1	0
BIST							

Bits 7-0 Hardwired to 00H because Savage4 does not support BIST

**Base Address 0 (PCI10) (Mapping 0 or 1) (Rev. A)**

Read/Write Address: 000 8010H

PCI Index: 12H (high) 10H (low)

Power-On Default: 7000 0000H

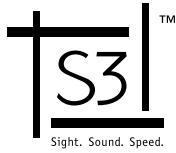
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	PREF = 0	TYPE =00	MSI = 0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 0								0	0	0	0	0	0	0	0

Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)

Bits 2-1 TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)

Bit 3 PREF - Prefetchable  
0 = Does not meet the prefetchable requirements (hardwired)





Bits 31-4 BASE ADDRESS 0

Value = Base address for accessing Savage4 registers via memory-mapped I/O

This field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for MMIO register accesses.

Setting all bits to 0s disables this base address register.

**Base Address 0 (PCI10) (Mapping 0 or 1) (Rev. B)**

Read/Write Address: 000 8010H  
Power-On Default: 7000 0000H

PCI Index: 12H (high) 10H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	PREF = 0	TYPE = 00		MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 0													0	0	0

- Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)
- Bits 2-1 TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3 PREF - Prefetchable  
0 = Does not meet the prefetchable requirements (hardwired)
- Bits 31-4 BASE ADDRESS 0

Value = Base address for accessing Savage4 registers via memory-mapped I/O

This field provides for address relocation. The programmable bits map to system address bits 31-19. All other address bits (18-4) return 0 on read to specify that Savage4 requires a 512K address space for MMIO register accesses.

Setting all bits to 0s disables this base address register.

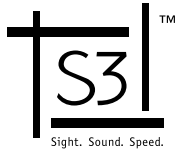
**Base Address 1 (PCI14) (Mapping 0, CRB0\_7 = 1) (Rev. A and B)**

Read/Write Address: 000 8014H  
Power-On Default: 6000 0008H

PCI Index: 16H (high) 14H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	PREF = 1	TYPE = 00		MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 1					0	0	0	0	0	0	0	0	0	0	0

- Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)
- Bits 2-1 TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3 PREF - Prefetchable  
1 = Meets the prefetchable requirements (hardwired)



Bits 31-4 BASE ADDRESS 1

Value = Base address for linear access of the Savage4 frame buffer, tiled addressing apertures and BCI command data transfers

This field provides for address relocation. The programmable bits map to system address bits 31-27. All other address bits (26-4) return 0 on read to specify that Savage4 requires a 128-MByte address space for linear addressing, tiled addressing apertures and BCI command data. Note that writes to CR59\_7-3 will also update this field, so if the linear addressing base address is being changed (testing only), the programmer must do a read-modify-write to ensure that this field is not changed.

Setting all bits to 0s disables this base address register.

**Base Address 1 (PCI14) (Mapping 1, CRB0\_7 = 0) (Rev. A)**

Read/Write Address: 000 8014H  
Power-On Default: 6000 0008H

PCI Index: 16H (high) 14H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0		0	0	0	0	0	PREF = 1	TYPE = 00		MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 1								0	0	0	0	0	0	0	0

- Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)
- Bits 2-1 TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3 PREF - Prefetchable  
1 = Meets the prefetchable requirements (hardwired)
- Bits 31-4 BASE ADDRESS 1

Value = Base address for linear access of the first 16 MBytes of the Savage4 frame buffer

This field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for the lower 16 MBytes of linear addressing. Note that writes to CR59\_7-0 will also update this field, so if the linear addressing base address is being changed (old linear addressing only, it should never be changed with new linear addressing), the programmer must do a read-modify-write to ensure that this field is not changed.

Setting all bits to 0s disables this base address register.

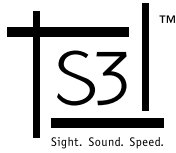
**Base Address 1 (PCI14) (Mapping 1, CRB0\_7 = 0) (Rev. B)**

Read/Write Address: 000 8014H  
Power-On Default: 6000 0008H

PCI Index: 16H (high) 14H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	PREF = 1	TYPE = 00		MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 1								0	0	0	0	0	0	0	0

- Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)



- Bits 2-1 TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3 PREF - Prefetchable  
1 = Meets the prefetchable requirements (hardwired)
- Bits 31-4 BASE ADDRESS 1

Value = Base address for linear access of the of the Savage4 frame buffer

This field provides for address relocation. The programmable bits map to system address bits 31-25. All other address bits (24-4) return 0 on read to specify that Savage4 requires a 32-MByte address space for linear addressing. Note that writes to CR59\_7-1 will also update this field, so if the linear addressing base address is being changed (old linear addressing only, it should never be changed with new linear addressing), the programmer must do a read-modify-write to ensure that this field is not changed.

Setting all bits to 0s disables this base address register.

**Base Address 2 (PCI18) (Mapping 1, CRB0\_7 = 0) (Rev. A)**

Read/Write Address: 000 8018H  
Power-On Default: 6800 0008H

PCI Index: 1AH (high) 18H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0		0	0	0	0	0	PREF = 1		TYPE =00	MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 2									0	0	0	0	0	0	0

- Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)
- Bits 2-1 TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3 PREF - Prefetchable  
1 = Meets the prefetchable requirements (hardwired)
- Bits 31-4 BASE ADDRESS 2

Value = Base address for linear access of the second 16 MBytes of the Savage4 frame buffer

This field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for the upper 16 MBytes of linear addressing.

Setting all bits to 0s disables this base address register.

**Base Address 2 (PCI18) (Mapping 1, CRB0\_7 = 0) (Rev. B)**

Read/Write Address: 000 8018H  
Power-On Default: 6800 0008H

PCI Index: 1AH (high) 18H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0		0	0	0	0	0	PREF = 1		TYPE =00	MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 2									0	0	0	0	0	0	0

- Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)

- Bits 2-1      TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3         PREF - Prefetchable  
1 = Meets the prefetchable requirements (hardwired)
- Bits 31-4    BASE ADDRESS 2

Value = Base address for tiled address aperture 0

for This field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for tile address aperture 0.

Setting all bits to 0s disables this base address register.

**Base Address 3 (PCI1C) (Mapping 1, CRB0\_7 = 0) (Rev A)**

Read/Write                      Address: 000 801CH  
Power-On Default: 6200 0008H

PCI Index: 1EH (high) 1CH (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0		0	0	0	0	0	PREF = 1	TYPE =00		MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 3										0	0	0	0	0	0

- Bit 0         MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)
- Bits 2-1    TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3         PREF - Prefetchable  
1 = Meets the prefetchable requirements (hardwired)
- Bits 31-4    BASE ADDRESS 3

Value = Base address for tiled address aperture 0

for This field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for tile address aperture 0.

Setting all bits to 0s disables this base address register.

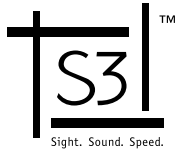
**Base Address 3 (PCI1C) (Mapping 1, CRB0\_7 = 0) (Rev B)**

Read/Write                      Address: 000 801CH  
Power-On Default: 6200 0008H

PCI Index: 1EH (high) 1CH (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0		0	0	0	0	0	PREF = 1	TYPE =00		MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 3										0	0	0	0	0	0

- Bit 0         MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)
- Bits 2-1    TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)



Bit 3      PREF - Prefetchable  
           1 = Meets the prefetchable requirements (hardwired)

Bits 31-4    BASE ADDRESS 3

Value = Base address for tiled address aperture 1

For this field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for tile address aperture 1.

Setting all bits to 0s disables this base address register.

**Base Address 4 (PCI20) (Mapping 1, CRB0\_7 = 0) (Rev. A)**

Read/Write                      Address: 000 8020H  
 Power-On Default: 6300 0008H

PCI Index: 22H (high) 20H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	0	0	0	0	0		0	0	0	0	0	PREF = 1	TYPE =00		MSI = 0		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
BASE ADDRESS 4											0	0	0	0	0	0	0

Bit 0      MSI - Memory Space Indicator  
           0 = Base registers map into memory space (hardwired)

Bits 2-1    TYPE - Type of Address Relocation  
           00 = Locate anywhere in 32-bit address space (hardwired)

Bit 3      PREF - Prefetchable  
           1 = Meets the prefetchable requirements (hardwired)

Bits 31-4    BASE ADDRESS 4

Value = Base address for tiled address aperture 1

For this field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for tile address aperture 1.

Setting all bits to 0s disables this base address register.

**Base Address 4 (PCI20) (Mapping 1, CRB0\_7 = 0) (Rev. B)**

Read/Write                      Address: 000 8020H  
 Power-On Default: 6300 0008H

PCI Index: 22H (high) 20H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	0	0	0	0	0		0	0	0	0	0	PREF = 1	TYPE =00		MSI = 0		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
BASE ADDRESS 4											0	0	0	0	0	0	0

Bit 0      MSI - Memory Space Indicator  
           0 = Base registers map into memory space (hardwired)

Bits 2-1    TYPE - Type of Address Relocation  
           00 = Locate anywhere in 32-bit address space (hardwired)

Bit 3      PREF - Prefetchable  
           1 = Meets the prefetchable requirements (hardwired)

Bits 31-4 BASE ADDRESS 4

Value = Base address for tiled address aperture 2

For This field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for tile address aperture 2.

Setting all bits to 0s disables this base address register.

**Base Address 5 (PCI24) (Mapping 1, CRB0\_7 = 0) (Rev. A)**

Read/Write Address: 000 8024H  
Power-On Default: 6400 0008H

PCI Index: 26H (high) 24H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0		0	0	0	0	0	PREF = 1	TYPE = 00		MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 5								0	0	0	0	0	0	0	0

- Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)
- Bits 2-1 TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3 PREF - Prefetchable  
1 = Meets the prefetchable requirements (hardwired)
- Bits 31-4 BASE ADDRESS 5

Value = Base address for tiled address aperture 2

For This field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for tile address aperture 2.

Setting all bits to 0s disables this base address register.

**Base Address 5 (PCI24) (Mapping 1, CRB0\_7 = 0) (Rev. B)**

Read/Write Address: 000 8024H  
Power-On Default: 6400 0008H

PCI Index: 26H (high) 24H (low)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0		0	0	0	0	0	PREF = 1	TYPE = 00		MSI = 0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 5								0	0	0	0	0	0	0	

- Bit 0 MSI - Memory Space Indicator  
0 = Base registers map into memory space (hardwired)
- Bits 2-1 TYPE - Type of Address Relocation  
00 = Locate anywhere in 32-bit address space (hardwired)
- Bit 3 PREF - Prefetchable  
1 = Meets the prefetchable requirements (hardwired)

**Bits 31-4      BASE ADDRESS 5**

Value = Base address for tiled address aperture 3

for This field provides for address relocation. The programmable bits map to system address bits 31-24. All other address bits (23-4) return 0 on read to specify that Savage4 requires a 16-MByte address space for tile address aperture 3.

Setting all bits to 0s disables this base address register.

**PCI Configuration Space Subsystem ID(PCI2C)**

Read Only                      Address: 2CH  
Power-On Default: 00000000H

This register is a shadow of CR81-CR84.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSYSTEM VENDOR ID															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUBSYSTEM ID															

Bits 15-0      SUBSYSTEM VENDOR ID  
Bits 31-16      SUBSYSTEM ID

**BIOS ROM Base Address (PCI30)**

Read/Write                      Address: 32H (high) 30H (low)  
Power-On Default: 000C 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	ADE
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIOS ROM BASE ADDRESS															

Bit 0              ADE - Address Decode Enable  
0 = Accesses to the BIOS ROM address space defined in this register are disabled  
1 = Accesses to the BIOS ROM address space defined in this register are enabled

Bits 15-1      Reserved  
Bits 31-16      BIOS ROM BASE ADDRESS

These are the upper 16 bits of the BIOS ROM address.

**Capabilities List Pointer (PCI34)**

Read/Write                      Address: 34H  
Power-On Default: DCH

This register value points to the offset of the first item in the capabilities list.

7	6	5	4	3	2	1	0
CAPABILITIES LIST POINTER							

Bits 7-0      CAPABILITIES LIST POINTER

This field is hardwired to DCH to point to the PCI power management capabilities list.

**Interrupt Line (PCI3C)**

Read/Write Address: 3CH

Power-On Default: 00H

This register contains interrupt line routing information written by the POST program during power-on initialization.

7	6	5	4	3	2	1	0
INTERRUPT LINE							

Bits 7-0 INTERRUPT LINE

**Interrupt Pin (PCI3D)**

Read Only Address: 3DH

Power-On Default: See below.

This register normally reads 01H to specify that INTA is the interrupt pin used. If CR36\_0 = 0, this register will read 00H to indicate that no interrupt should be assigned to this device.

7	6	5	4	3	2	1	0
INTERRUPT PIN							

Bits 7-0 INTERRUPT PIN

**Latency/Grant (PCI3E)**

Read Only Address: 3EH

Power-On Default: FF40H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXIMUM LATENCY								MINIMUM GRANT							

Bits 7-0 MINIMUM GRANT

Value = Length of burst period required in units of 250 ns (33 MHz clock)

Bits 15-8 MAXIMUM LATENCY

Value = Maximum latency of PCI access in units of 250 ns (33 MHz clock)

**Master Timeout Control (PCI40)**

Read Write Address: 40H

Power-On Default: 03H

7	6	5	4	3	2	1	0
R	R	R	R	MASTER TIMEOUT			

Bits 3-0 MASTER TIMEOUT

Value = # of PCI cycles the Savage4 master will wait for DEVSEL to be asserted before timing out

Bits 7-4 Reserved



**AGP Capability Identifier (PCI80)**

Read/Write Address: 80H (AGP offset + 00H)

Power-On Default: 00200002H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT POINTER								CAPABILITIES ID							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	MAJOR				MINOR			

Bits 7-0 CAPABILITIES ID

Hardwired to 02H to identify the capabilities list as pertaining to AGP.

Bits 15-8 NEXT POINTER

Hardwired to 00H.

Bits 19-16 MINOR

Hardwired to 0H to specify the minor revision level of the AGP interface specification to which this device conforms.

Bits 23-20 MAJOR

Hardwired to 2H to specify the major revision level of the AGP interface specification to which this device conforms.

Bits 31=24 Reserved

**AGP Status (PCI84)**

Read Only Address: 84H (AGP offset + 04H)

Power-On Default: 1F000x0xH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	SBA	R	R	R	R	R	R	RATE		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQUESTS SUPPORTED								R	R	R	R	R	R	R	R

Bits 2-0 RATE

This field indicates 1x, 2x and 4x clocking are supported. This applies to the AD and SBA busses. Bits 1-0 are hardwired to 11b. Bit 2 reflects the state of CRB0\_5. It will read 1 if 4x clocking is supported.

Bits 8-3 Reserved

Bit 9 SBA - Side Band Addressing

0 = Side band addressing not supported

1 = Side band addressing supported

The status of this bit is determined by the setting of CR70\_7.

Bits 23-10 Reserved

Bits 31-24 REQUESTS SUPPORTED ]

Hardwired to 1FH to indicate the maximum # of AGP command requests this device can manage.

**AGP Command (PCI88)**

Read/Write Address: 88H (AGP offset + 08H)

Power-On Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	SE	AE	R	R	R	R	R	DATA RATE		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQUEST DEPTH								R	R	R	R	R	R	R	R

Bits 2-0 DATA RATE  
 001 = 1x clocking desired  
 010 = 2x clocking desired  
 100 = 4x clocking desired

This field must be programmed to one of these three values. The master and target must be programmed for the same rate. 4x clocking can be selected only if PCI84\_2 = 1.

Bits 7-3 Reserved

Bit 8 AE - AGP Enable  
 0 = Master cannot initiate AGP operations  
 1 = Master can initiate AGP operations

The target must be enabled before the master. This bit is cleared by an AGP reset.

Bit 9 SE - SBA Enable  
 0 = Side band addressing disabled  
 1 = Side band addressing enabled

This bit can be set to 1 only if PCI84\_9 = 1.

Bits 23-10 Reserved

Bits 31-24 REQUESTS DEPTH

Value = Maximum # of pipelined operations the master is allowed to enqueue to the target

This value must be equal to or less than the value reported in the REQUESTS SUPPORTED field (AGP offset 4H\_31-24) of the target.

**AGP FIFO Status (PCI8C)**

Read Only Address: 8CH (AGP offset + 0CH)

Power-On Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	AB	OFF	OFE	DBF	DBE	RF	RE	R	R	CURRENT COMMAND					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 5-0 CURRENT COMMAND

Value = Current number of outstanding command in system side

Bits 7-6 Reserved

Bit 8 RE - Requester Empty Status  
 0 = AGP requester is empty  
 1 = AGP requester is not empty

Bit 9 RF - Requester Full Status  
 0 = AGP requester is not full  
 1 = AGP requester is full

- Bit 10 DBE - Data Buffer Empty Status  
0 = AGP data buffer is empty  
1 = AGP data buffer is not empty
- Bit 11 DBF - Data Buffer Full Status  
0 = AGP data buffer is not full  
1 = AGP data buffer is full
- Bit 12 OFE - Outstanding FIFO Empty Status  
0 = Outstanding FIFO is empty  
1 = Outstanding FIFO is not empty
- Bit 13 OFF - Outstanding FIFO Full Status  
0 = Outstanding FIFO is not full  
1 = Outstanding FIFO is full
- Bit 14 AB- AGP Master Busy  
0 = AGP master idle  
1 = AGP master busy
- Bits 31-15 Reserved

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**PCI Power Management Capability Identifier (PCIDC)**

Read Only                      Address: DCH (PM offset + 00H)  
Power-On Default: 0001H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT POINTER								CAPABILITIES ID							

- Bits 7-0 CAPABILITIES ID  
  
Hardwired to 01H to identify the capabilities list as pertaining to PCI power management.
- Bits 15-8 NEXT POINTER  
  
Hardwired to 80H to point to the AGP capabilities.

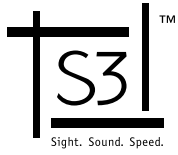
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**PCI Power Management Capabilities (PCIDE)**

Read Only                      Address: DEH (PM offset + 02H)  
Power-On Default: 0621H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	D2	D1	R	R	R	DSI	R	R	VERSION		

- Bits 2-0 VERSION  
  
Hardwired to 1H to indicate compliance with Revision 1.0 of the PCI Power Management Specification.
- Bits 4-3 Reserved
- Bit 5 DSI - Device Specific Initialization  
  
Hardwired to 1 to indicate a device specific initialization sequence is required following transition to the D0 uninitialized state.
- Bits 8-6 Reserved
- Bit 9 D1  
  
Hardwired to 1 to indicated support for the D1 power management state.
- Bit 10 D2  
  
Hardwired to 1 to indicated support for the D2 power management state.



Bits 15-11 Reserved

**PCI Power Management Control/Status (PCIE0)**

Read/Write Address: E0H (PM offset + 04H)  
Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	PS	

Bits 1-0 PS - Power State  
00 = D0  
01 = D1  
10 = D2  
11 = D3hot

The D2 state can only be enabled if CR42\_0 = 1.

Bits 15-2 Reserved

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## Section 7: 2D Graphics Engine Register Descriptions

These registers support the Enhanced mode 2D drawing commands.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined).

These registers can be accessed five different ways:

Access Method	Description
Old MMIO	Non-packed format. Accessed at Axxxx, where xxxx is the old I/O address (e.g. 9AE8) each register.
Old MMIO	Packed format starting at offset A8100.
New MMIO	Non-packed format compatible with old MMIO. Offset is 200 xxxx. The new MMIO offset is given in parentheses for each register.
New MMIO	Packed format starting at offset 200 8100. This is the preferred method for direct access.
BCI	Index defined for each register. This should normally be used by the drivers for all writes. Several registers do not have BCI indices and must be accessed directly.

The first two methods provide backwards compatibility for some drivers. The last two methods are more efficient and should be used by all new software. The registers are listed below in their original configurations and order, i.e., non-packed and by increasing old MMIO (AxxE8H) address. The MMxxxx designation will be out of order. Table 7-1 provides the correspondence between the various methods.

Only 16-bit reads of these registers are supported. 32-bit reads will return invalid data in the upper word. All the 16-bit registers will read correctly at their MMxxxx address. The 32-bit registers will require reads at the MMxxxx address and 2 bytes higher.

2D Graphics Engine Registers

Table 7-1. 2D Graphics Engine Registers Memory Mapping

Register Name	Old MMIO Address Axxxx (Hex)	Packed Old MMIO Address (Axxxx) or Packed New MMIO Address (000 xxxx) (Hex)	BCI Address (Hex)
Subsystem Status/Control	42E8	8504	N/A
FIFO Status	42EA	8508	N/A
Advanced Function Control	4AE8	850C	N/A
Wakeup		8510	N/A
Current Y, Current X	82E8, 86E8	8100, 8102	D0 (2x16-bit)
Destination Y, Destination X	8AE8, 8EE8	8108, 810A	D1 (2x16-bit)
Line Error Term	92E8	8110	D2 (16-bit)
Command	9AE8	8118	D3 (16-bit)
Short Stroke Vector	9EE8	811C	D4 (16-bit)
Background Color	A2E8	8120	D5 (32-bit)
Foreground Color	A6E8	8124	D6 (32-bit)
Write Mask	AAE8	8128	D7 (32-bit)
Read Mask	AEE8	812C	D8 (32-bit)
Color Compare	B2E8	8130	D9 (32-bit)
Background Mix, Foreground Mix	B6E8, BAE8	8134, 8136	DA (2x16-bit)
Top Scissors, Left Scissors	BEE8_1, BEE8_2	8138, 813A	DB (2x16-bit)
Bottom Scissors, Right Scissors	BEE8_3, BEE8_4	813C, 813E	DD (2x16-bit)
Pixel Control, Multi. Misc. 2	BEE8_A, BEE8_D	8140, 8142	DD (2x16-bit)
Multi. Misc. , Read Select	BEE8_E, BEE8_F	8144, 8146	DE (2x16-bit)
Minor Axis Count, Major Axis Count	BEE8_0, 96E8	8148, 814A	DF (2x16-bit)
Pixel Transfer	E2E8, E2EA	Range	N/A
Global Bitmap Descriptor 1	EAE8, EAEA	8168, 816A	E0 (32-bit)
Global Bitmap Descriptor 2	EEE8, EEEA	816C, 816E	E1 (32-bit)
Primary Bitmap Descriptor 1	F2E8, F2EA	8170, 8172	E2 (32-bit)
Primary Bitmap Descriptor 2	F6E8, F6EA	8174, 8176	E3 (32-bit)
Secondary Bitmap Descriptor 1	FAE8, F8EA	8178, 817A	E4 (32-bit)
Secondary Bitmap Descriptor 2	FEE8, FEEA	817C, 817E	E5 (32-bit)

2D Graphics Engine Registers

**Subsystem Status Register (MM8504)**

Read Only                      Address: 42E8H (8504H)

Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	LPB	BCI	CFE	CFF	BFE	BFF	GE BSY	VSY INT
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	CB LT	CB UT

- Bit 0            VSY INT - Vertical Sync Interrupt Status  
0 = No interrupt  
1 = Interrupt generated if enabled
- Bit 1            GE BSY - 2D Graphics Engine Busy Interrupt Status  
0 = No interrupt  
1 = Interrupt generated if enabled
- Bit 2            BFF - BFIFO Full Interrupt Status  
0 = No interrupt  
1 = Interrupt generated if enabled
- Bit 3            BFE - BFIFO Empty Interrupt Status  
0 = No interrupt  
1 = Interrupt generated if enabled
- Bit 4            CFF - CFIFO Full Interrupt Status  
0 = No interrupt  
1 = Interrupt generated if enabled
- Bit 5            CFE - CFIFO Empty Interrupt Status  
0 = No interrupt  
1 = Interrupt generated if enabled
- Bit 6            BCI - BCI Interrupt Status  
0 = No Interrupt  
1 = Interrupt generated if enabled
- Bit 7            LPB - LPB Interrupt Status  
0 = No Interrupt  
1 = Interrupt generated if enabled
- Bits 15-8       Reserved
- Bit 16           CB UT - Command Overflow Buffer Upper Threshold Interrupt Status  
0 = No Interrupt  
1 = Interrupt generated if enabled
- Bit 17           CB LT - Command Overflow Buffer Lower Threshold Interrupt Status  
0 = No Interrupt  
1 = Interrupt generated if enabled
- Bits 31-18      Reserved

2D Graphics Engine Registers

**Subsystem Control Register (MM8504)**

Write Only                      Address: 42E8H (8504H)

Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GE SR	CRE ENB	CFE ENB	BFF ENB	CFE ENB	CFF ENB	GE BSY	VSY ENB	R	BCI CLR	CFE CLR	CFF CLR	BFE CLR	BFF CLR	GEB CLR	VSY CLR
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	LT ENB	UT ENB	R	R	R	R	R	R	R	LT CLR	UT CLR

- Bit 0            VSY CLR - Clear Vertical Sync Interrupt Status  
0 = No change  
1 = Clear
- Bit 1            GEB CLR - Clear 2D/3D Graphics Engine Busy Interrupt Status  
0 = No change  
1 = Clear
- Bit 2            BFF CLR - Clear BFIFO Full Interrupt Status  
0 = No change  
1 = Clear
- Bit 3            BFE CLR - Clear BFIFO Empty Interrupt Status  
0 = No change  
1 = Clear
- Bit 4            CFO CLR - Clear CFIFO Full Interrupt Status  
0 = No change  
1 = Clear
- Bit 5            CFE CLR - Clear CFIFO Empty Interrupt Status  
0 = No change  
1 = Clear
- Bit 6            BCI CLR - Clear BCI Interrupt Status  
0 = No change  
1 = Clear
- Bit 7            LPB CLR - Clear LPB Interrupt Status  
0 = No change  
1 = Clear
- Bit 8            VSY ENB - Vertical Sync Interrupt Enable  
0 = Disable  
1 = Enable if CR32\_4 = 1
- Bit 9            GE BSY - 2D/3D Graphics Engine Busy Interrupt Enable  
0 = Disable  
1 = Enable if CR32\_4 = 1
- Bit 10          BFF ENB - BIU FIFO Full Interrupt Enable  
0 = Disable  
1 = Enable if CR32\_4 = 1
- Bit 11          BFE ENB - BIU FIFO Empty Interrupt Enable  
0 = Disable  
1 = Enable if CR32\_4 = 1
- Bit 12          CFF ENB - Command FIFO Full Interrupt Enable  
0 = Disable  
1 = Enable if CR32\_4 = 1
- Bit 13          CFE ENB - Command FIFO Empty Interrupt Enable  
0 = Disable  
1 = Enable if CR32\_4 = 1



2D Graphics Engine Registers

- Bit 14      BCI ENB - BCI Interrupt Enable  
0 = Disable  
1 = Enable if CR32\_4 = 1
- Bit 15      GE SR - 2D Graphics Engine Software Reset  
0 = No effect  
1 = Software reset (ORed with CR66\_1)
- Bit 16      UT CLR - Clear Command Overflow Buffer Upper Threshold Interrupt  
0 = No change  
1 = Clear
- Bit 17      LT CLR - Clear Command Overflow Buffer Lower Threshold Interrupt  
0 = No change  
1 = Clear
- Bits 23-18    Reserved
- Bit 24      UT ENB - Command Overflow Buffer Upper Threshold Interrupt Enable  
0 = Disable  
1 = Enable if CR32-4 = 1  
  
The upper threshold is defined in MM48C10\_15-0.
- Bit 25      LT ENB - Command Overflow Buffer Lower Threshold Interrupt Enable  
0 = Disable  
1 = Enable if CR32-4 = 1  
  
The lower threshold is defined in MM48C10\_31-16.
- Bits 31-26    Reserved

**FIFO Status Register (MM8508)**

Read Only                      Address: 42EAH (8508H)  
Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CFE	OBF	RBF	WBF	R	R	R	R	CFE	OBE	RBE	WBE
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Bit 0      WBE - Command Write Buffer (on chip) Empty Status  
0 = Not empty  
1 = Empty
- Bit 1      RBE - Command Read Buffer (on chip) Empty Status  
0 = Not empty  
1 = Empty
- Bit 2      OBE - Command Overflow Buffer (frame buffer) Empty Status  
0 = Not empty  
1 = Empty
- Bit 3      CFE - Command FIFO (CFIFO) Empty Status  
0 = Not empty  
1 = Empty
- Bits 7-4    Reserved
- Bit 8      WBF - Command Write Buffer (on chip) Full Status  
0 = Not full  
1 = Full

2D Graphics Engine Registers

- Bit 9        RBF - Command Read Buffer (on chip) Full Status  
0 = Not full  
1 = Full
- Bit 10      OBF - Command Overflow Buffer (frame buffer) Full Status  
0 = Not Full  
1 = Full
- Bit 11      CFF - Command FIFO (CFIFO) Full Status  
0 = Not full  
1 = Full
- Bits 31-12   Reserved

**Advanced Function Control Register (MM850C)**

Read/Write                      Address: 4AE8H (850CH)  
Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	GC	GECD		R	R	R	LA	R	PL	R	E23
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Bit 0        E23 - Enable 2D/3D Engine Operation  
0 = Disable 2D/3D Engine operation (VGA operation)  
1 = Enable 2D/3D Engine operation  
  
This bit must only be programmed during screen off (SR1\_5 = 1) or during the vertical retrace period. Setting SR1\_5 to 1 may take up to 3 HSYNCs to take effect. This bit has the same function as CR66\_0. Programming one of these bits also changes affects the other bit.
- Bit 1        Reserved
- Bit 2        PL - Enhanced Mode Pixel Length  
0 = 4 bits/pixel enhanced mode  
1 = 8 or more bits/pixel enhanced mode  
CR50\_5-4 are used to differentiate between 8-, 16- and 32-bit pixel lengths.
- Bit 3        Reserved
- Bit 4        LA - Enable Linear Addressing  
0 = Disable linear addressing  
1 = Enable linear addressing  
  
This bit is ORed with bit 4 of CR58 and is equivalent to it.
- Bits 7-5     Reserved
- Bits 9-8     GECD - 2D Graphics Engine Clock Divide  
00 = MCLK/2  
01 = MCLK/4  
10 = MCLK  
11 = MCLK
- Bits 15-10   Reserved
- Bit 16      IC - Internal Clock Select  
0 = Internal clock is 66 MHz except for the system bus interface and LPB functions  
1 = Internal clock is 33 MHz
- Bits 31-17   Reserved

**Wakeup Register (MM8510)**

Read/Write Address: 8510H  
 Power-On Default: 000C 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	WU
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 WU - Wake Up  
 0 = Chip function disabled  
 1 = Chip function enabled  
  
 This bit is ORed with 3C3H\_0.

**Current Y-Position Register (MM8100)**

Read/Write Address: 82E8H (8100H) BCI: D0H (lower word)  
 Power-On Default: Undefined

For line draws (solid, textured, short stroke or polyline), rectangle draws and image transfers, writing to this register defines the vertical screen coordinate at which the first pixel will be drawn. For BitBLTs, this is the vertical coordinate for the upper left hand corner of the source. For PatBLTs, this is the vertical coordinate of the upper left hand corner of the off-screen pattern. Reading this register produces the current vertical drawing coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CURRENT Y-POSITION											

Bits 11-0 CURRENT Y-POSITION  
 Bits 15-12 Reserved

2D Graphics Engine Registers

**Current X-Position Register (MM8102)**

Read/Write Address: 86E8H (8102H)

BCI: D0H (upper word)

Power-On Default: Undefined

For line draws (solid, textured, short stroke or polyline), rectangle draws and image transfers, writing to this register defines the horizontal screen coordinate at which the first pixel will be drawn. For BitBLTs, this is the horizontal coordinate for the upper left hand corner of the source. For PatBLTs, this is the horizontal coordinate of the upper left hand corner of the off-screen pattern. Reading this register produces the current horizontal drawing coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CURRENT X-POSITION											

Bits 11-0 CURRENT X-POSITION

Bits 15-12 Reserved

**Destination Y-Position/Axial Step Constant Register (MM8108)**

Read/Write Address: 8AE8H (8108H) BCI: D1H (lower word)

Power-On Default: Undefined

For BitBLTs and PatBLTs, this register defines the vertical position for the top of the destination rectangle. For solid and textured line draws, this is axial step constant used in the definition of the line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DESTINATION Y-POSITION											

Bits 11-0 DESTINATION Y-POSITION

Bits 15-12 Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER AXIAL STEP CONSTANT													

Axial Step Constant =  $2 * (\min(|dx|, |dy|))$  In other words, when drawing a line from point A to point B, determine the change in the X coordinate from A to B and the change in the Y coordinate from A to B. Take the smaller of the two changes and multiply its absolute value by 2.

Bits 13-0 LINE PARAMETER AXIAL STEP CONSTANT

Bits 15-14 Reserved

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2D Graphics Engine Registers

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**Destination X-Position/Diagonal Step Constant Register (MM810A)**

Read/Write Address: 8EE8H (810AH)

BCI: D1H (upper word)

Power-On Default: Undefined

For BitBLTs and PatBLTs, this register defines the horizontal position for the left side of the destination rectangle. For solid and textured line draws, this is diagonal step constant used in the definition of the line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DESTINATION X-POSITION											

Bits 11-0 DESTINATION X-POSITION

Bits 15-12 Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER DIAGONAL STEP CONSTANT													

Diagonal Step Constant =  $2 * [\min(|dx|, |dy|) - \max(|dx|, |dy|)]$ . See the Destination Y-Position/Axial Step Constant (MM8108) register for an explanation of the terms used in this equation.

Bits 13-0 LINE PARAMETER DIAGONAL STEP CONSTANT

Bits 15-14 Reserved

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**Line Error Term Register (MM8110)**

Read/Write Address: 92E8H (8110H)

BCI: D2H (lower word only)

Power-On Default: Undefined

This register specifies the initial error term for solid and textured line draws.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER/ERROR TERM													

Error Term =  $2 * \min(|dx|, |dy|) - \max(|dx|, |dy|) - 1$  if the starting X < the ending X

Error Term =  $2 * \min(|dx|, |dy|) - \max(|dx|, |dy|)$  if the starting X  $\geq$  the ending X

See the Destination Y-Position/Axial Step Constant (MM8108) register for an explanation of the terms used in these equations.

Bits 13-0 LINE PARAMETER/ERROR TERM

Bits 15-14 Reserved

**Drawing Command Register (MM8118)**

Write Only                      Address: 9AE8H (8118H)

BCI: D3H

Power-On Default: Undefined

This register specifies the drawing command and a number of associated control parameters. MM8144\_9 must be set to 1 to access the upper 16 bits of this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CMD-TYPE			BS	R	BUS SIZE			WY	DRWG-DIR			DS	DT	LP	PM	= 1
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	R	R	R	R	R	R	R	R	R	R	R	DESTBD		SPBD		

- Bit 0            This bit must always be programmed to 1.
- Bit 1            PM - Select Across the Plane Pixel Mode  
0 = Single pixel transferred at a time  
1 = Multiple pixels transferred at a time (across the plane mode)
- Bit 2            LP - Last Pixel Off  
0 = Last pixel of line or vector draw will be drawn  
1 = Last pixel of line or vector draw will not be drawn
- Bit 3            DT - Select Radial Direction Type  
0 = x-y (axial)  
1 = Radial
- Bit 4            DY - Draw Pixel  
0 = Move the current position only - don't draw  
1 = Draw pixel(s)
- Bits 7-5        DRWG-DIR - Select Drawing Direction

In the following table, radial drawing angle is measured counterclockwise from the X axis. For axial line draws, the line is drawn from left to right or a +X and from right to left for a -X, down for a +Y and up for a -Y. X or Y maj specifies the longest axis.

7-5	Radial (bit 3 = 1)	x-y (Axial - bit 3 = 0)
000	0°	-Y,X maj,-X
001	45°	-Y,X maj,+X
010	90°	-Y,Y maj,-X
011	135°	-Y,Y maj,+X
100	180°	+Y,X maj,-X
101	225°	+Y,X maj,+X
110	270°	+Y,Y maj,-X
111	315°	+Y,Y maj,+X

- Bit 8            WY - Wait for CPU Data  
0 = Use 2D Graphics Engine-based data  
1 = Wait for data to be transferred to or from the CPU
- Bits 10-9      BUS SIZE - Select image write bus transfer width  
00 = 8 bits  
01 = 16 bits  
10 = 32 bits. All doubleword bits beyond the image rectangle width are discarded. Each line starts with a fresh doubleword. The current drawing position ends up one pixel below the lower left hand corner of the image rectangle.  
11 = 32 bits. This setting applies only to image transfers across the plane (each bit transferred is converted to a pixel). Only bits from the end of the line width to the next byte boundary are discarded. Data for the next line begins with the next byte. The current drawing position ends up one pixel to the right of the top right corner of the image rectangle.

This parameter applies only to image write data.



2D Graphics Engine Registers

Bits 7-5 DRWG-DIR.- Select Drawing Direction (measured counterclockwise from the X axis)  
 000 = 0°  
 001 = 45°  
 010 = 90°  
 011 = 135°  
 100 = 180°  
 101 = 225°  
 110 = 270°  
 110 = 315°

Bits 15-8 These bits duplicate bits 7-0 to define the second short stroke vector.

**Background Color Register (MM8120)**

Read/Write Address: A2E8H (8120H) BCI: D5H  
 Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BACKGROUND COLOR															

Bits 31-0 BACKGROUND COLOR

**Foreground Color Register (MM8124)**

Read/Write Address: A6E8H (8124H) BCI: D6H  
 Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOREGROUND COLOR															

Bits 31-0 FOREGROUND COLOR

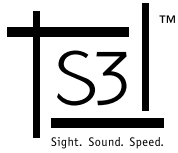
**Bitplane Write Mask Register (MM8128)**

Read/Write Address: AAE8H (8128H) BCI: D7H  
 Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE WRITE MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT-PLANE WRITE MASK															

Bits 31-0 BIT-PLANE WRITE MASK  
 If bit i = 0, bitplane i is not updated  
 If bit i = 1, bitplane i is updated





**Bitplane Read Mask Register (MM812C)**

Read/Write Address: AEA8H (812CH)

BCI: D8H

Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE READ MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT-PLANE READ MASK															

Bits 31-0 BIT-PLANE READ MASK  
 If bit i = 0, bitplane i is not used as a data source  
 If bit i = 1, bitplane i is used as a data source

**Color Compare Register (MM8130)**

Read/Write Address: B2E8H (8130H)

BCI: D9H

Power-On Default: Undefined

This register contains the color value that is compared against the current bitmap color if the color compare option is turned on by setting bit 8 of the Pixel Control (MM8140) to 1. Bit 7 of the Pixel Control register determines whether a match or a non-match results in a pixel update.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPARISON COLOR WITH SOURCE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMPARISON COLOR WITH SOURCE															

Bits 31-0 COMPARISON COLOR WITH SOURCE

## 2D Graphics Engine Registers

### Background and Foreground Mix Registers (MM8134, MM8136)

Read/Write Address: B6E8H (8134H) (Background)

Address: BAE8H (8136H) (Foreground)

BCI: DAH (lower word)

BCI: DAH (upper word)

Power-On Default: Undefined

This register has two different definitions, depending on the setting of bit 15.

#### Bit 15 = 0 (16 ROPs definition)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RT	R	R	R	R	R	R	R	R	CLR SRC	R					
												MIX TYPE			

Bits 3-0 MIX TYPE - Select Mix Type

In the general case, a new color is defined. A logical operation such as AND or OR is then performed between it and the current bitmap color. If the bitplane to be written is enabled, the result of this logical "mix" is written to the bitmap as the new pixel color. The following table shows the mix types available (! = logical NOT).

0000	!current	1000	!current OR !new
0001	logical zero	1001	current OR !new
0010	logical one	1010	!current OR new
0011	leave current as is	1011	current OR new
0100	!new	1100	current AND new
0101	current XOR new	1101	!current AND new
0110	!(current XOR new)	1110	current AND !new
0111	new	1111	!current AND !new

Bit 4 Reserved

Bits 6-5 CLR SRC - Select Color Source  
 00 = Background Color register is the color source  
 01 = Foreground Color register is the color source  
 10 = CPU data (the CPU is the color source)  
 11 = Display memory (the display memory is the color source)

Bits 14-7 Reserved

Bit 15 RT - ROP Type  
 0 = 16 ROPs register definition  
 1 = 256 ROPs register definition

#### Bit 15 = 1 (256 ROPs definition)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RT	R	R	R	CLR PAT	CLR SRC										
												MIX TYPE			

Bits 7-0 MIX TYPE - Select Mix Type

256 raster operations according the Microsoft definition

Bits 9-8 CLR-SRC - Select Color Source  
 00 = Background Color register is the color source  
 01 = Foreground Color register is the color source  
 10 = CPU data (the CPU is the color source)  
 11 = Display memory (the display memory is the color source)

2D Graphics Engine Registers

Bits 11-10 CLR-PAT - Select Color Pattern  
 00 = Background Color register is the color source  
 01 = Foreground Color register is the color source  
 10 = Reserved  
 11 = 8x8 pattern from display memory

The source and pattern colors cannot both be from display memory.

Bits 14-12 Reserved

Bit 15 RT - ROP Type  
 0 = 16 ROPs register definition  
 1 = 256 ROPs register definition

**Read Register Data Register**

Read Only Address: BEE8H  
 Power-On Default: Undefined

Note: This register (and the Read Select Register, BEE8, Index F) are only used with non-packed MMIO addressing. The various indexes can be read directly at their packed new MMIO addresses. The pipeline issue described below does not apply to this case.

A read of this register produces a read of the register specified by bits 3-0 of the Read Register Select (BEE8H, Index 0FH) register. Each read of BEE8H causes the read index (bits 3-0 of BEE8H, Index 0FH) to increment by one. Registers BEE8H, Indices 0H to 0EH, 9AE8H and 42E8H can thus be rapidly read by successive reads from BEE8H.

Note: Writes to the BEE8H registers (except the read index register, Index 0FH) are pipelined. Therefore, to correctly read back a write to one of these registers, issue an engine command and wait for engine idle. Next, write the desired register index to BEE8H, Index 0FH and read the data from BEE8H.

The BEE8H registers are written directly by writing to BEE8H with the appropriate register index in bits 15-12.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

**Minor Axis Pixel Count Register (MM8148)**

Write Only Address: BEE8H, Index 0 (8148H) BCI: DFH (lower word)  
 Power-On Default: Undefined

This register specifies the height for rectangles, image transfers, BitBLTs and PatBLTs.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	RECTANGLE HEIGHT											

Bits 11-0 RECTANGLE HEIGHT

Value = (number of pixels in the height of the rectangle) - 1

Bits 15-12 INDEX = 0H

2D Graphics Engine Registers

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**Top Scissors Register (MM8138)**

Write Only Address: BEE8H, Index 1 (8138H)

BCI: DBH (lower word)

Power-On Default: Undefined

This register specifies the top of the clipping rectangle. It is the lowest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	CLIPPING TOP LIMIT											

Bits 11-0 CLIPPING TOP LIMIT

Bits 15-12 INDEX = 1H

**Left Scissors Register (MM813A)**

Write Only Address: BEE8H, Index 2 (813AH)

BCI: DBH (upper word)

Power-On Default: Undefined

This register specifies the left side of the clipping rectangle. It is the lowest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	CLIPPING LEFT LIMIT											

Bits 11-0 CLIPPING LEFT LIMIT

Bits 15-12 INDEX = 2H

**Bottom Scissors Register (MM813C)**

Write Only Address: BEE8H, Index 3 (813CH)

BCI: DCH (lower word)

Power-On Default: Undefined

This register specifies the bottom of the clipping rectangle. It is the highest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	CLIPPING BOTTOM LIMIT											

Bits 11-0 CLIPPING BOTTOM LIMIT

Bits 15-12 INDEX = 3H

Bits 15-11 Reserved

**Right Scissors Register (MM813E)**

Write Only Address: BEE8H, Index 4 (813EH)

BCI: DCH (upper word)

Power-On Default: Undefined

This register specifies the right side of the clipping rectangle. It is the highest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	CLIPPING RIGHT LIMIT											

Bits 11-0 CLIPPING RIGHT LIMIT

Bits 15-12 INDEX = 4H

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2D Graphics Engine Registers

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**Pixel Control Register (MM8140)**

Write Only Address: BEE8H, Index AH (8140H)

BCI: DDH (lower word)

Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	R	R	R	R	DT-EX-SRC 1 0		R	R	R	R	R	R

Bits 5-0 Reserved

Bits 7-6 DT-EX-SRC - Select Mix Register  
00 = Foreground Mix register is always selected  
01 = Reserved  
10 = CPU data determines Mix register selected  
11 = Display memory current value determines Mix register selected

Bits 11-8 Reserved

Bits 15-12 INDEX = 0AH

**Multifunction Control Miscellaneous 2 Register (MM8142)**

Write Only Address: BEE8H, Index DH (8142H)

BCI: DDH (upper word)

Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
=1	=1	=0	=1	=0	=0	=0	=0	=0	SRC-BASE		=0	DST=BASE			

Bits 2-0 DST-BASE - Destination Base Address  
000 = First destination memory address is in the 1st MByte of display memory  
001 = First destination memory address is in the 2nd MByte of display memory  
010 = First destination memory address is in the 3rd MByte of display memory  
011 = First destination memory address is in the 4th MByte of display memory

This field supersedes bits 1-0 of BEE8H, Index E if any of these 3 bits are set to 1.

Bit 3 Reserved

Bits 6-4 SRC-BASE - Source Base Address  
000 = First source memory address is in the 1st MByte of display memory  
001 = First source memory address is in the 2nd MByte of display memory  
010 = First source memory address is in the 3rd MByte of display memory  
011 = First source memory address is in the 4th MByte of display memory

This field supersedes bits 3-2 of BEE8H, Index E if any of these three bits are set to 1.

Bit 7 Reserved

Bits 9-8 WFE - Wait for FIFO Empty  
10 = Wait for write FIFO empty between each drawing

All other values have no effect. Bits 7-0 of this register must be programmed to FFH for this to be effective.

Bits 11-10 Reserved

Bits 15-12 INDEX = 0DH

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2D Graphics Engine Registers

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**Multifunction Control Miscellaneous (MM8144)**

Write Only                      Address: BEE8H, Index EH (8144H)

BCI: DEH (lower word)

Power-On Default: Undefined

Software must initialize this register appropriately before the 2D Graphics Engine is used. See the description for BEE8H, read only, for the required two step register update sequence.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				DC	R	32B	ENB CMP	SRC NE	R	EXT CLIP	RS F	SRC-BA 21 20	DEST-BA 21 20		
1	1	1	0												

Bits 1-0        DEST-BA 21 20 - Destination Base Address Bits 21-20  
00 = First destination memory address is in the 1st MByte of display memory  
01 = First destination memory address is in the 2nd MByte of display memory  
10 = First destination memory address is in the 3rd MByte of display memory  
11 = First destination memory address is in the 4th MByte of display memory

This field is superseded by bits 2-0 of BEE8H, Index D if any of the BEE8H Index D bits is set to 1.

Bits 3-2        SRC-BA 21 20 - Source Base Address Bits 21-20  
00 = First source memory address is in the 1st MByte of display memory  
01 = First source memory address is in the 2nd MByte of display memory  
10 = First source memory address is in the 3rd MByte of display memory  
11 = First source memory address is in the 4th MByte of display memory

This field is superseded by bits 6-4 of BEE8H Index D if any of the BEE8H Index D bits is set to 1.

Bit 4            RSF - Select Upper Word in 32 Bits/Pixel Mode  
0 = Selects lower 16 bits for accesses to 32-bit registers in 32 bpp mode  
1 = Selects upper 16 bits for accesses to 32-bit registers in 32 bpp mode

Bit 5            EXT CLIP - Enable External Clipping  
0 = Only pixels inside the clipping rectangle are drawn  
1 = Only pixels outside the clipping rectangle are drawn

Bit 6            Reserved

Bit 7            SRC NE - Don't Update Bitmap if Source Not Equal to Color Compare Color  
0 = Don't update current bitmap if the Color Compare (B2E8) register value is equal to the color value of the source bitmap  
1 = Don't update current bitmap if the Color Compare (B2E8) register value is not equal to the color value of the source bitmap

This bit is only active if bit 8 of this register is set to 1.

Bit 8            ENB CMP - Enable Color Compare  
0 = Disable color comparison  
1 = Enable color comparison

Bit 9            32B - Enable 32-bit Register Write  
0 = 16-bit 2D Engine register access  
1 = 32-bit 2D Engine register access

Bit 10          Reserved

Bit 11          DC - Disable Clipping  
0 = Clipping defined by scissors registers  
1 = Clipping disabled

Bits 15-12     INDEX = 0EH

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**2D Graphics Engine Registers**


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**Read Register Select Register (MM8146)**

Write Only                      Address: BEE8H, Index FH, (8146H)  
 Power-On Default: Undefined

BCI: DEH (upper word)

Although this register has a BCI address, it will never be used with BCI because it deals only with register reads using non-packed MMIO.

<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
1	1	1	1	R	R	R	R	R	R	R	R	READ-REG-SEL			

Bits 3-0              READ-REG-SEL - Read Register Select

When BEE8H is read, the value returned is determined by this read register index according to the following:

- 0000 = BEE8H, Index 0H
- 0001 = BEE8H, Index 1H
- 0010 = BEE8H, Index 2H
- 0011 = BEE8H, Index 3H
- 0100 = BEE8H, Index 4H
- 0101 = BEE8H, Index 0AH
- 0110 = BEE8H, Index 0EH
- 0111 = 9AE8H (Bits 15-13 of the read data are forced to 0)
- 1000 = 42E8H (Bits 15-12 of the read data are forced to 0)
- 1001 = Reserved
- 1010 = BEE8H, Index 0DH

The read register index increments by one with each reading of BEE8H.

Bits 11-4            Reserved

Bits 15-12          INDEX = 0FH

---

**Major Axis Pixel Count Register (MM814A)**

Read/Write                      Address: 96E8H (814AH)  
 Power-On Default: Undefined

BCI: DFH (upper word)

This register specifies the length (in pixels) of the major (longest) axis for solid and textured lines and the width for rectangles, image transfers, BitBLTs and PatBLTs.

<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
R	R	R	R	RECTANGLE WIDTH/LINE PARAMETER MAX											

Bits 11-0            RECTANGLE WIDTH/LINE PARAMETER MAX

The value is the number of pixels along the major axis - 1.

Bits 15-12          Reserved

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2D Graphics Engine Registers

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**Global Bitmap Descriptor 1 Register (MM8168)**

Read/Write Address: EAE8H (8168H)

BCI: E0H

Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OFFSET															

Bits 31-0      OFFSET

Value = Starting address of the bitmap (in bytes)

**Global Bitmap Descriptor 2 Register (MM816C)**

Read/Write Address: EEE8 (816CH)

BCI: E1H

Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	STRIDE									BE	BLE	R	BDS
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	BD	R	R	TF	COLOR DEPTH								

Bit 0      BDS - Bitmap Descriptor Size  
0 = 32 bits (this register only)  
1 = 64 bits (includes global bitmap descriptor 1)

The 64-bit descriptor must be enabled when memory tiling is used.

Bit 1      Reserved

Bit 2      BLE - Big/Little Endian Addressing for Image Writes  
0 = Little endian  
1 = Big endian

Bit 3      BE - BCI Enable (2D Engine only)  
0 = BCI disabled  
1 = BCI enabled

Bits 12-4      STRIDE

Value = Stride of the bitmap (in pixels \* 16)

Bits 15-13      Reserved

Bits 23-16      COLOR FORMAT

Value = Binary coding of the color depth in bits/pixel

Bits 25-24      TF - Tile Format  
00 = Linear  
01 = Reserved  
10 = 16 bits  
11 = 32 bits

Bits 27-26      Reserved



2D Graphics Engine Registers

Bit 28 BD - Block Write Disable  
 0 = Block write enabled  
 1 = Block write disabled

Bits 31-29 Reserved

**Primary Bitmap Descriptor 1 Register (MM8170)**

Read/Write Address: F2E8H (8170H)  
 Power-On Default: Undefined

BCI: E2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OFFSET															

Bits 31-0 OFFSET

Value = Starting address of the bitmap (in bytes)

**Primary Bitmap Descriptor 2 Register (MM8174)**

Read/Write Address: F6E8H (8174H)  
 Power-On Default: Undefined

BCI: E3H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
STRIDE																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	R	R	BD	TILE FORMAT				COLOR DEPTH								

Bits 15-0 STRIDE

Value = Stride of the bitmap (in pixels)

If the value = 0, the bitmap is linear.

Bits 22-16 COLOR DEPTH

Value = Binary coding of the color depth in bits/pixel

For example, 8 bits/pixel is coded 0000 1000b. The value must be 8, 16 or 32. 15 bits/pixel is coded as 16.

Bits 27-24 TILE FORMAT

0000 = Linear  
 0010 = 16 bits  
 0011 = 32 bits

All other values are reserved.

Bit 28 BD - Block Write Disable  
 0 = Block write enabled  
 1 = Block write disabled

Bits 31-29 Reserved

**Secondary Bitmap Descriptor 1 Register (MM8178)**

Read/Write Address: FAE8H (8178H)

BCI: E4H

Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OFFSET															

Bits 31-0      OFFSET

Value = Starting address of the bitmap (in bytes)

**Secondary Bitmap Descriptor 2 Register (MM817C)**

Read/Write Address: FEE8H (817CH)

BCI: E5H

Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
STRIDE																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	R	R	BD	TILE FORMAT				COLOR DEPTH								

Bits 15-0      STRIDE

Value = Stride of the bitmap (in pixels)

If the value = 0, the bitmap is linear.

Bits 22-16      COLOR DEPTH

Value = Binary coding of the color depth in bits/pixel

For example, 8 bits/pixel is coded 0000 1000b. The value must be 8, 16 or 32. 15 bits/pixel is coded as 16.

Bits 27-24      TILE FORMAT

- 0000 = Linear
- 0010 = 16 bits
- 0011 = 32 bits

All other values are reserved.

Bit 28          BD - Block Write Disable

- 0 = Block write enabled
- 1 = Block write disabled

Bits 31-29      Reserved

## Section 8: Streams Processor Register Descriptions

Many Streams Processor registers will normally be written via the BCI. Direct new MMIO access for these registers and those without BCI addresses is also available. The register identifier MMxxxx means that the register is memory mapped at offset 200 xxxx from the base address.

---

### Primary Stream Control Register (MM8180)

Read/Write Address: 8180H  
 Power-on Default: 00000000H

BCI: A0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PSFC			R	PSIDF			R	R	R	R	R	R	R	R

Bits 23-0 Reserved

Bits 26-24 PSIDF - Primary Stream Input Data Format  
 000 = RGB-8 (CLUT)  
 001 = 4-bit Alpha RGB (AAAxxxx.8.8.8)  
 010 = Reserved  
 011 = KRGB-16 (1.5.5.5)  
 100 = Reserved  
 101 = RGB-16 (5.6.5)  
 110 = RGB-24 (8.8.8) - This mode is not accelerated.  
 111 = XRGB-32 (X.8.8.8)

Bit 27 Reserved

Bits 30-28 PSFC - Primary Stream Filter Characteristics  
 000 = Primary stream not filtered  
 001 = Primary stream stretched 2x both horizontally and vertically using replication  
 010 = Primary stream stretched 2x horizontally using interpolation and 2x vertically using replication

Other values reserved

Bit 31 Reserved

---

### Color/Chroma Key Control Register (MM8184)

Read/Write Address: 8184H  
 Power-on Default: 00000000H

BCI: A1H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G/U/Cb KEY (LOW)								B/V/Cr KEY (LOW)							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	CKI	KC	R	RGB CC			R/Y KEY (LOW)							

Bits 7-0 B/V/Cr key value (lower bound for chroma)

Bits 15-8 G/U/Cb key value (lower bound for chroma)

Bits 23-16 R/Y key value (lower bound for chroma)

Streams Processor Registers

- Bits 26-24 RGB CC - RGB Color Comparison Precision
  - 000 = Compare bit 7 of RGB (compare red bit 7's, green bit 7's and blue bit 7's)
  - 001 = Compare bits 7-6 of RGB
  - 010 = Compare bits 7-5 of RGB
  - 011 = Compare bits 7-4 of RGB
  - 100 = Compare bits 7-3 of RGB
  - 101 = Compare bits 7-2 of RGB
  - 110 = Compare bits 7-1 of RGB
  - 111 = Compare bits 7-0 of RGB
- Bit 27 Reserved
- Bit 28 KC - Key Control
  - 0 = Extract key data from input stream key bit (if present). (KRGB-16, 1.5.5.5 only)  
If the K bit is 0, the pixel from the other stream is used (transparent). If the K bit is 1, the key bit streams pixel is used (opaque)
  - 1 = Enable color or chroma keying for all modes other than KRGB-16
- Bit 29 CKI - Color Keying on Index
  - 0 = Color keying based on color value
  - 1 = Color keying based on comparison of color index value with value specified in MM8184\_7-0.
- Bits 31-30 Reserved

**Genlocking Control Register (MM8188)**

Read/Write Address: 8188H  
Power-on Default: 00000000H

BCI: A2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHARACTER CLOCKS BETWEEN VSYNCS															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GL	HD	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Bits 15-0 CHARACTER CLOCKS BETWEEN VSYNCS (Read Only)
  - Value = [Character clocks from T1 to T2]/16
  - Where:
    - T1 = The falling edge of VSYNC (VSYNC active high) or the rising edge of VSYNC (VSYNC active low)
    - T2 = The rising edge of the LPB VSYNC input.
- Bits 29-16 Reserved
- Bit 30 HD - HDTV Function Enable
  - 0 = HDTV function disabled
  - 1 = HDTV function enabled

When this bit is set to 1, DCLK (pixel clock) is driven out on the ROMA3 pin (to an HDTV encoder), and the OVERLAY signal is driven out on the ROMA2 pin to control an analog MUX such that primary stream data is displayed when OVERLAY is low and high resolution RGB data is displayed when OVERLAY is high.
- Bit 31 GL - Genlock Support Enable
  - 0 = Genlock support disabled
  - 1 = Genlock support enabled

Setting this bit to 1 enables the counter described in bits 15-0 of this register.

Streams Processor Registers

**Secondary Stream Control Register (MM8190)**

Read/Write Address: 8190H  
 Power-on Default: 00000000H

BCI: A4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	R	R	R	SOURCE HORIZONTAL PIXEL SIZE												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
LOI	R	R	R	R	SDIF				R	R	R	R	R	HDM		

Bits 11-0 SOURCE HORIZONTAL PIXEL SIZE

Value = # of pixels/line in the source image

Updating of this field is controlled by CR66\_4 and CR51\_7.

Bits 15-12 Reserved

Bits 18-16 HDM - Horizontal Downscaling Mode

- 010 = 4:1
- 011 = 8:1
- 100 = 16:1
- 101 = 32:1
- 110 = 64:1
- 111 = Reserved

All other values result in no scaling. Use MM8198 for scaling ratios between 1:1 and 2:1. Downscaling is only valid for YCbCr formats.

Bits 23-19 Reserved

Bits 26-24 SDIF - Secondary Stream Input Data Format

- 000 = CbYCrY-16 (4.2.2)
- 001 = YCbCr-16 (4.2.2)
- 010 = YUV-16 (4.2.2)
- 011 = KRGB-16 (1.5.5.5)
- 100 = YCbCr-16 (4.2.0)
- 101 = RGB-16 (5.6.5)
- 110 = RGB-24 (8.8.8)
- 111 = XRGB-32 (X.8.8.8)

Updating of this field is controlled by CR66\_4 and CR51\_7.

Bits 30-27 Reserved

Bit 31 LOI - Luma-only Interpolation

- 0 = All YUV values interpolated when vertical filtering enabled
- 1 = Only Y (luma) values interpolated when vertical filtering enabled

**Chroma Key Upper Bound Register (MM8194)**

Read/Write Address: 8194H  
 Power-on Default: 00000000H

BCI: A5H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U/Cb KEY (UPPER)								V/Cr KEY (UPPER)							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	Y KEY (UPPER)							

Bits 7-0 V/Cr key value (upper bound)

Bits 15-8 U/Cb key value (upper bound)

Bits 23-16 Y key value (upper bound)

Streams Processor Registers

Bits 31-24 Reserved

**Secondary Stream Horizontal Scaling Register (MM8198)**

Read/Write Address: 8198H  
Power-on Default: 00000000H

BCI: A6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HORIZONTAL SCALING RATIO															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HORIZONTAL INITIAL VALUE															

Bits 15-0 HORIZONTAL SCALING RATIO

Value = (# of pixels/line in source image)/(# of pixels/line in scaled image)

This value has a format of D.FFFFFFFFFFFFFFFF, and FFFFFFFFFFFFFFFF is the fraction resulting from the value calculation. The decimal part D is always 0 when upscaling is enabled. The D bit is set to 1 for horizontal downscaling, with the fractional part defining the degree of downscaling. The maximum value is all 1's, resulting in approximately 2:1 downscaling. Downscaling is only valid for YCbCr formats. The horizontal downscaling mode for ratios larger than 2:1 is defined via MM8190\_18-16. Updating of this field is controlled by CR66\_5 and CR51\_7.

Bits 31-16 HORIZONTAL INITIAL VALUE

Value = S.FFFFFFFFFFFFFFFF

where S is always 0 (positive value) and FFFFFFFFFFFFFFFF is the fractional part, which can be programmed from 000 0000 0000 0000b to 111 1111 1111 1111b. Updating of this field is controlled by CR66\_4 and CR51\_7.

**Color Adjustment Register (MM819C)**

Read/Write Address: 819CH  
Power-on Default: 00000000H

BCI: A7H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BCE	R	R	CONTRAST					BRIGHTNESS								
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
HSE	R	R	HUE/SAT 2					R	R	R	HUE/SAT 1					

Bits 7-0 BRIGHTNESS - Brightness Control

Value = BBBB BBBB

where BBBB BBBB is the brightness adjustment factor (0 - 255). The larger the number, the greater the brightness.

Bits 12-8 CONTRAST- Contrast Control

Value = C.CCCC

This is the contrast adjustment, which can vary from 0 (0.0000) to 1.9375 (1.1111).

Bits 14-13 Reserved

Bits 15 BCE - Brightness and Contrast Enable

0 = Brightness and contrast control disabled  
1 = Brightness and contrast control enabled

This control should be enabled only for YUV/YCbCr secondary stream formats and must be disabled for RGB secondary stream formats.

Streams Processor Registers

Bits 20-16 HUE/SAT 1 - Hue and Saturation Factor 1

Value = SF.FFF

where S is the sign bit (1 = negative) and F.FFF is the factor [SAT \* cosine A]. SAT is the saturation, which can vary from -1.875 (10001) to 1.875 (01111) and A is the hue angle, the cosine of which can vary from -1 to +1. The value is in 2's complement format.

Bits 23-21 Reserved

Bits 28-24 HUE/SAT 2 - Hue and Saturation Factor 2

Value = SF.FFF

where S is the sign bit (1 = negative) and F.FFF is the factor [SAT \* sine A]. SAT is the saturation, which can vary from -1.875 (10001) to 1.875 (01111) and A is the hue angle, the sine of which can vary from -1 to +1.

Bits 30-29 Reserved

Bit 31 HSE - Hue and Saturation Control Enable

0 = Hue and saturation control disabled  
1 = Hue and saturation control enabled

This control should be enabled only for YUV/YCbCr secondary stream formats and must be disabled for RGB secondary stream formats.

**Blend Control Register (MM81A0)**

Read/Write Address: 81A0H  
Power-on Default: 00000000H

BCI: A8H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	R	R	KP			R	R	R	R	R	KS			R	R	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	R	R	R	R	COMP MODE			R	R	R	R	R	R	R	R	R

Bits 1-0 Reserved

Bits 4-2 Ks

Value = secondary stream blend coefficient

Updating of this field is controlled by CR66\_4 and CR51\_7.

Bits 9-5 Reserved

Bits 12-10 Kp

Value = primary stream blend coefficient

Updating of this field is controlled by CR66\_4 and CR51\_7.

Bits 23-13 Reserved

Streams Processor Registers

- Bits 26-24 Compose Mode  
 000 = Secondary stream opaque overlay on primary stream  
 001 = Primary stream opaque overlay on secondary stream  
 010 = Dissolve,  $[P_p \times K_p + P_s \times (8 - K_p)]/8$ , ignore  $K_s$   
 011 = Fade,  $[P_p \times K_p + P_s \times K_s]/8$ , where  $K_p + K_s$  must be  $\leq 8$   
 100 = Alpha blending, (higher alpha means greater primary stream dominance on pixel color)  
 101 = Color key on primary stream (secondary stream overlay on primary stream)  
 110 = Color or chroma key on secondary stream (primary stream overlay on secondary stream)  
 111 = Reserved

When this field is programmed, the value does not take effect until the next VSYNC.

- Bits 31-27 Reserved

**Primary Stream Frame Buffer Address 0 Register (MM81C0)**

Read/Write Address: 81C0H BCI: B0H  
 Power-on Default: 00000000H

If a primary stream is enabled, this register specifies the starting address in the frame buffer. Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIMARY BUFFER ADDRESS 0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBR		TBW		R	VS	PBS	PRIMARY BUFFER ADDRESS 0								

- Bits 24-0 PRIMARY BUFFER ADDRESS 0  
 Value = Primary stream frame buffer starting address 0  
 This value must be quadword aligned.
- Bit 25 PBS - Primary Stream Buffer Select  
 0 = Primary frame buffer starting address 0 (MM81C0\_24-0) used for the primary stream  
 1 = Primary frame buffer starting address 1 (MM81C4\_24-0) used for the primary stream
- Bit 26 VS - VSYNC Off Mode  
 0 = VSYNC off mode off  
 1 = VSYNC off mode on  
 When this bit is set, the display buffer can be changed (bit 25 of this register) between VSYNCs.
- Bit 27 Reserved
- Bits 29-28 TBW – Triple Buffering Writes (Rev. B)  
 00 = Triple buffering not used  
 01 = Next write is to buffer 0  
 10 = Next write is to buffer 1  
 11 = Next write is to buffer 2
- Bits 31-30 TBR – Triple Buffering Read (Rev. B)  
 00 = Triple buffering not used  
 01 = Next read is from buffer 0  
 10 = Next read is from buffer 1  
 11 = Next read is from buffer 2



Streams Processor Registers

**Primary Stream Frame Buffer Address 1 Register (MM81C4)**

Read/Write Address: 81C4H BCI: B1H  
 Power-on Default: Undefined

If the primary stream is double buffered, this register specifies the starting address in the frame buffer for the second buffer. Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
PRIMARY BUFFER ADDRESS 1																		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
R	R	R	R	R	R	R	PRIMARY BUFFER ADDRESS 1											

Bits 24-0 PRIMARY BUFFER ADDRESS 1  
 Value = Primary stream frame buffer starting address 1  
 This value must be quadword aligned.

Bits 31-25 Reserved

**Primary Stream Stride Register (MM81C8)**

Read/Write Address: 81C8H BCI: B2H  
 Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	PRIMARY STREAM STRIDE												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ET	BPP	PRIMARY STREAM TILE OFFSET													

Bits 12-0 PRIMARY STREAM STRIDE  
 Value = byte offset of vertically adjacent pixels in the primary stream buffer(s)  
 If double or triple buffering is used, the stride must be the same for all buffers.

Bits 15-13 Reserved

Bits 29-16 PRIMARY STREAM TILE OFFSET  
 Value = [Scan line width in bytes/128 bytes per tile] x 256 QWords/tile  
 This is the # of QWords from a given position in one tile to the same position in the tile immediately below. This applies only to 16-line tiles.

Bit 30 BPP - Tiling Bits/Pixel  
 0 = 16 bits/pixel tile format  
 1 = 32 bits/pixel tile format

This bit applies when tiling is enabled via bit 31 of this register. The power-on default value is 0.  
 Bit 31 ET - Enable Tiling  
 0 = Primary stream tiling off  
 1 = Primary stream tiling on  
 The power-on default value is 0.

Streams Processor Registers

**Secondary Stream Multiple Buffer/LPB Support Register (MM81CC)**

Read/Write Address: 81CCH

BCI: B3H

Power-on Default: xxxxxx00H

Bits 7-0 of this register control double or triple buffering, depending on the setting of bit 7. The bit definitions are different for each case, so two sets of definitions are provided. The bit diagram following is for the triple buffering case. This register is only programmed when double or triple buffering of the secondary stream with LPB input is required.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	BS	LST	LSL	LIS		SBS		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

The following definitions for bits 6-0 apply when double buffering is selected (bit 7 of this register cleared to 0).

Bit 0 Reserved

Bits 2-1 SBS - Secondary Stream Buffer Select

- 00 = Secondary frame buffer starting address 0 (MM81D0\_22-0) used for the secondary stream
- 01 = Secondary frame buffer starting address 1 (MM81D4\_22-0) used for the secondary stream
- 10 = Secondary frame buffer starting address 0 (MM81D0\_22-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C\_22-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4\_22-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10\_22-0) used for the LPB input stream. Which alternative applies is determined by LPB starting address register selected by bit 4 of this register
- 11 = Secondary frame buffer starting address 0 (MM81D0\_22-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10\_22-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4\_22-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C\_22-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bit 4 of this register

Bit 3 Reserved

Bit 4 LIS - LPB Input Buffer Select

- 0 = LPB frame buffer starting address 0 (MMFF0C\_21-0) used for the LPB input
- 1 = LPB frame buffer starting address 1 (MMFF10\_21-0) used for the LPB input

This bit selects the starting address for writing LPB data into the frame buffer. When the value programmed to this bit takes effect is determined by the setting of bit 5 of this register. This bit can be toggled at the completion of writing all the data for a frame to the frame buffer via bit 6 of this register

Bit 5 LSL - LPB Input Buffer Select Loading

- 0 = The value programmed into bit 4 of this register takes effect immediately
- 1 = The value programmed into bit 4 of this register takes effect at the next end of frame (completion of writing all the data for a frame into the frame buffer)

Bit 6 LST - LPB Input Buffer Select Toggle

- 0 = End of frame (completion of writing all the data for a frame into the frame buffer) has no effect on the setting of bit 4 of this register
- 1 = End of frame causes the setting of bit 4 of this register to toggle

## Streams Processor Registers

The following definitions for bits 6-0 apply when triple buffering is selected (bit 7 of this register set to 1).

- Bits 2-0** SBS - Secondary Stream Buffer Select  
 000 = Secondary frame buffer starting address 0 (MM81D0\_22-0) used for the secondary stream  
 010 = Secondary frame buffer starting address 1 (MM81D4\_22-0) used for the secondary stream  
 0x1 = Secondary frame buffer starting address 2 (MM8308\_22-0) used for the secondary stream  
 10x = Secondary frame buffer starting address 0 (MM81D0\_22-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C\_22-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4\_22-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10\_22-0) used for the LPB input stream OR secondary frame buffer starting address 2 (MM8308\_22-0) used for the secondary stream and LPB frame buffer starting address 2 (MMFF38\_22-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bits 4-3 of this register  
 11x = Secondary frame buffer starting address 0 (MM81D0\_22-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10\_22-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4\_22-0) used for the secondary stream and LPB frame buffer starting address 2 (MMFF38\_22-0) used for the LPB input stream OR secondary frame buffer starting address 2 (MM8308\_22-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C\_22-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bits 4-3 of this register
- Bits 4-3** LIS - LPB Input Buffer Select  
 00 = LPB frame buffer starting address 0 (MMFF0C\_22-0) used for the LPB input  
 01 = LPB frame buffer starting address 2 (MMFF38\_22-0) used for the LPB input  
 10 = LPB frame buffer starting address 1 (MMFF10\_22-0) used for the LPB input  
 11 = Reserved
- This bit selects the starting address for writing LPB data into the frame buffer. When the value programmed to this bit takes effect is determined by the setting of bits 6-5 of this register. This selected address can be rotated among at the completion of writing all the data for a frame to the frame buffer via bit 6 of this register
- Bit 5** LSL - LPB Input Buffer Select Loading  
 0 = The value programmed into bits 4-3 of this register takes effect immediately  
 1 = The value programmed into bits 4-3 of this register takes effect as specified by bit 6 of this register
- Bit 6** LST - LPB Input Buffer Select Toggle  
 0 = The value programmed into bits 4-3 of this register takes effect after all data has been written to the frame buffer for the current frame. The buffer selection remains unchanged until changed by programming.  
 1 = The value programmed into bits 4-3 of this register takes effect after all data has been written to the frame buffer for the current frame. At the end of each successive frame, the buffer selection will shift to the next higher buffer (or wrap from buffer 2 to buffer 0).
- This bit is only effective when bit 5 of this register = 1.
- Bit 7** BS - Buffering Select  
 0 = Double buffering  
 1 = Triple buffering
- Bits 31-8** Reserved

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Streams Processor Registers

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**Secondary Stream Frame Buffer Address 0 Register (MM81D0)**

Read/Write Address: 81D0H

BCI: B4H

Power-on Default: Undefined

If a secondary stream is enabled, this register specifies the starting address in the frame buffer. Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
SECONDARY BUFFER ADDRESS 0																		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 0											

Bits 24-0 SECONDARY BUFFER ADDRESS 0

Value = Secondary stream frame buffer starting address 0

This value must be quadword aligned. In YCbCr420 mode, this is the Y base address.

Bits 31-25 Reserved

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**Secondary Stream Frame Buffer Address 1 Register (MM81D4)**

Read/Write Address: 81D4H

BCI: B5H

Power-on Default: Undefined

If the secondary stream is double buffered, this register specifies the starting address in the frame buffer for the second buffer. Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
SECONDARY BUFFER ADDRESS 1																		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 1											

Bits 24-0 SECONDARY BUFFER ADDRESS 1

Value = Secondary stream frame buffer starting address 1

This value must be quadword aligned.

Bits 31-25 Reserved

Streams Processor Registers

**Secondary Stream Stride Register (MM81D8)**

Read/Write Address: 81D8H  
 Power-on Default: Undefined

BCI: B6H

Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBP	R	R	SECONDARY STREAM STRIDE												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SST	R	SECONDARY STREAM TILE OFFSET													

Bits 12-0 SECONDARY STREAM STRIDE

Value = byte offset of vertically adjacent pixels in the secondary stream buffer(s)

If double or triple buffering is used, the stride must be the same for all buffers. In YCbCr420 mode, this field is the secondary stream Y stride.

Bits 14-13 Reserved

Bit 15 SBP - Streams Bits/Pixel  
 0 = 16 bpp  
 1 = 32 bpp

This bit is only required when tiling is enabled.

Bits 29-16 SECONDARY STREAM TILE OFFSET

14-bit Value = [Scan line width in bytes/128 bytes per tile] x 256 QWords/tile

This is the # of QWords from a given position in one tile to the same position in the tile immediately below. This applies only to 16-line tiles.

Bit 30 Reserved

Bit 31 SST - Secondary Stream Tiling  
 0 = Secondary stream tiling off  
 1 = Secondary stream tiling on

**Secondary Stream Vertical Scaling Register (MM81E0)**

Read/Write Address: 81E0H  
 Power-on Default: 00000000H

BCI: B8H

Updating of this register is controlled via CR66\_5 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL SCALING RATIO															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
VERT SCALE RATIO															

Bits 19-0 VERTICAL SCALING RATIO

Value = (# of lines in source image)/(# of lines in scaled image)

This value has a format of DDDDD.FFFFFFFFFFFFFFFF, and FFFFFFFFFFFFFFFF is the fraction resulting from the value calculation. For upscaling, the decimal part DDDDD is always 0. For downscaling, the maximum value is all 1's, resulting in a maximum downscaling of approximately 32:1. Downscaling is only valid for YCbCr modes.

Bits 31-20 Reserved

Streams Processor Registers

**Secondary Stream Vertical Initial Value (MM81E4)**

Read/Write Address: 81E4H

BCI: B9H

Power-on Default: 00000000H

Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL INITIAL VALUE 1															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL INITIAL VALUE 2															

Bits 15-0 VERTICAL INITIAL VALUE 1

Value = S.FFFFFFFFFFFFFFFF

where S is the sign bit (1 = negative) and FFFFFFFFFFFFFFFF is the fractional part. The value can range from 1.000 0000 0000 0001b (-0.9999694824) to 0.111 1111 1111 1111b (0.9999694824).

Bits 31-16 VERTICAL INITIAL VALUE 2

Value = S.FFFFFFFFFFFFFFFF

where S is the sign bit (1 = negative) and FFFFFFFFFFFFFFFF is the fractional part. The value can range from 1.000 0000 0000 0001b (-0.9999694824) to 0.111 1111 1111 1111b (0.9999694824).

**Secondary Stream Source Line Count (MM81E8)**

Read/Write Address: 81E8H

BCI: BAH

Power-on Default: 00000000H

Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVI	R	R	R	R	SOURCE LINE COUNT										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 SOURCE LINE COUNT

Value = # of lines in the source image (before scaling)

Bits 14-11 Reserved

Bit 15 EVI - Enable Vertical Interpolation

0 = Line duplication

1 = Enable vertical interpolation

This bit is effective when a non-zero scaling ratio is programmed in MM81E0\_15-0. Line duplication is used when the line buffer is too small or when there is insufficient bandwidth for interpolation.

Bits 31-16 Reserved

Streams Processor Registers

**Streams FIFO Register (MM81EC)**

Read/Write Address: 81ECH  
 Power-on Default: 00006000H

BCI: BBH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFIFO THRESHOLD					SFIFO THRESHOLD					FIFO ALLOCATION					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	PFT

Bits 4-0

**STREAMS FIFO ALLOCATION**

The following apply only when vertical interpolation is disabled (MM81E8\_15 = 0).  
 00010 = Primary Stream (PS) = 64 slots, Secondary Stream (SS) = 204 slots  
 11110 = PS = 204 slots (Enhanced mode only)

All other values are reserved.

When vertical interpolation is enabled (MM81E8\_15 = 1), FIFO allocation is fixed as follows:

For all values: PS = 64 slots, SS = 64 slots, Line Buffer = 204 slots

Each slot holds one quadword.

Bits 10-5

**SECONDARY FIFO THRESHOLD**

Value = (Number of secondary FIFO slots)/F

where F = 1 if the secondary stream is using the 64-slot FIFO and F=4 if the secondary stream is using the 204-slot FIFO.

When the secondary FIFO empties down to this value, an internal signal is generated requesting re-filling of the secondary FIFO. This value must be less than or equal to the secondary stream FIFO size specified in bits 4-0.

Bits 16-11

**PRIMARY FIFO THRESHOLD**

Value = (Number of primary FIFO slots)/F

where F = 1 if the primary stream is using the 64-slot FIFO and F=4 if the primary stream is using the 204-slot FIFO.

When the primary FIFO empties down to this value, an internal signal is generated requesting re-filling of the primary FIFO. This value must be less than or equal to the primary stream FIFO size specified in bits 4-0.

Bits 31-17

Reserved

**Primary Stream Window Start Coordinates Register (MM81F0)**

Read/Write Address: 81F0H  
 Power-on Default: Undefined

BCI: BCH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	PRIMARY STREAM Y-START										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	PRIMARY STREAM X-START										

Bits 10-0

**PRIMARY STREAM Y-START**

Value = Screen line number +1 of the first line of the primary stream window

Bits 15-11

Reserved

Streams Processor Registers

Bits 26-16 PRIMARY STREAM X-START

Value = Screen pixel number +1 of the first pixel of the primary stream window

Bits 31-27 Reserved

**Primary Stream Window Size Register (MM81F4)**

Read/Write Address: 81F4H  
Power-on Default: Undefined

BCI: BDH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	PRIMARY STREAM HEIGHT										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	PRIMARY STREAM WIDTH										

Bits 10-0 PRIMARY STREAM HEIGHT

Value = Number of lines displayed in the primary stream window

Bits 15-11 Reserved

Bits 26-16 PRIMARY STREAM WIDTH

Value = Number of pixels -1 displayed in each line in the primary stream window

Bits 31-27 Reserved

**Secondary Window Start Coordinates Register (MM81F8)**

Read/Write Address: 81F8H  
Power-on Default: Undefined

BCI: BEH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SECONDARY STREAM Y-START										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	SECONDARY STREAM X-START										

Bits 10-0 SECONDARY STREAM Y-START

Value = Screen line number +1 of the first line of the secondary stream window

Bits 15-11 Reserved

Bits 26-16 SECONDARY STREAM X-START

Value = Screen pixel number +1 of the first pixel of the secondary stream window

Bits 31-27 Reserved



Streams Processor Registers

**Secondary Window Size (MM81FC)**

Read/Write Address: 81FCH  
 Power-on Default: 0000000H

BCI: BFH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SECONDARY STREAM HEIGHT										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	SECONDARY STREAM WIDTH										

Bits 10-0 SECONDARY STREAM HEIGHT

Value = Number of lines displayed in the secondary stream window

Bits 15-11 Reserved

Bits 26-16 SECONDARY STREAM WIDTH

Value = Number of pixels -1 displayed in each line in the primary stream window

Bits 31-27 Reserved

**Primary Stream FIFO Monitoring 0 Register (MM8200)**

Read/Write Address: 8200H  
 Power-on Default: 0000000H

BCI: C0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	PRIMARY STREAM FIFO LOW WATERMARK							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	PRIMARY STREAM FIFO HIGH WATERMARK							

Bits 7-0 PRIMARY STREAM FIFO LOW WATERMARK

Value = # of entries in the primary stream FIFO

When the number of FIFO entries is less than this value, the Lower Counter value (MM8210\_15-0) is incremented by one at each FIFO read strobe.

Bits 15-0 Reserved

Bits 23-16 PRIMARY STREAM FIFO HIGH WATERMARK

Value = # of entries in the primary stream FIFO

When the number of FIFO entries is greater than this value, the Higher Counter value (MM8210\_31\_16) is incremented by one at each FIFO write strobe.

Bits 31-24 Reserved

Streams Processor Registers

**Secondary Stream FIFO Monitoring 0 Register (MM8204)**

Read/Write Address: 8204H

BCI: C1H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	SECONDARY STREAM FIFO LOW WATERMARK							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	SECONDARY STREAM FIFO HIGH WATERMARK							

Bits 7-0 SECONDARY STREAM FIFO LOW WATERMARK

Value = # of entries in the secondary stream FIFO

When the number of FIFO entries is less than this value, the Lower Counter value (MM8214\_15-0) is incremented by one at each FIFO read strobe.

Bits 15-0 Reserved

Bits 23-16 SECONDARY STREAM FIFO HIGH WATERMARK

Value = # of entries in the secondary stream FIFO

When the number of FIFO entries is greater than this value, the Higher Counter value (MM8214\_31\_16) is incremented by one at each FIFO write strobe.

Bits 31-24 Reserved

**Secondary Stream Frame Buffer Cb Block Address Register (MM8208)**

Read/Write Address: 8208H

BCI: C2H

Power-on Default: Undefined

In YCbCr420 mode, this is the buffer address for the Cb data. Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY BUFFER Cb BLOCK ADDRESS															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	SECONDARY BUFFER Cb BLOCK ADDRESS								

Bits 24-0 SECONDARY BUFFER Cb/U BLOCK ADDRESS

Value = Secondary stream frame buffer Cb block starting address

This value must be quadword aligned.

Bits 31-25 Reserved

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Streams Processor Registers

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**Secondary Stream Frame Buffer Cr Block Address Register (MM820C)**

Read/Write Address: 820CH  
Power-on Default: Undefined

BCI: C3H

In YCbCr420 mode, this is the buffer address for the Cr data. Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
SECONDARY BUFFER Cr BLOCK ADDRESS																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
R	R	R	R	R	R	R	SECONDARY BUFFER Cr BLOCK ADDRESS										

Bits 24-0 SECONDARY BUFFER Cr BLOCK ADDRESS

Value = Secondary stream frame buffer Cr block starting address

This value must be quadword aligned.

Bits 31-25 Reserved

---

**Primary Stream FIFO Monitoring 1 Register (MM8210)**

Read/Write Address: 8210H  
Power-on Default: 00000000H

BCI: C4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIMARY STREAM FIFO LOWER COUNTER															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRIMARY STREAM FIFO HIGHER COUNTER															

Bits 15-0 PRIMARY STREAM FIFO LOWER COUNTER

Value = The number of primary stream FIFO read strobes that occurred when the number of FIFO entries was less than the low watermark specified in MM8200\_7-0

The counter stops incrementing when it reaches 8000H. It is reset by writing 0000H to it.

Bits 31-16 PRIMARY STREAM FIFO HIGHER COUNTER

Value = The number of primary stream FIFO write strobes that occurred when the number of FIFO entries was greater than the high watermark specified in MM8200\_23-16

The counter stops incrementing when it reaches 8000H. It is reset by writing 0000H to it.

---

**Secondary Stream FIFO Monitoring 1 Register (MM8214)**

Read/Write Address: 8214H  
Power-on Default: 00000000H

BCI: C5H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY STREAM FIFO LOWER COUNTER															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SECONDARY STREAM FIFO HIGHER COUNTER															

Bits 15-0 SECONDARY STREAM FIFO LOWER COUNTER

Value = The number of secondary stream FIFO read strobes that occurred when the number of FIFO entries was less than the low watermark specified in MM8204\_7-0

The counter stops incrementing when it reaches 8000H. It is reset by writing 0000H to it.

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Streams Processor Registers

## Bits 31-16 SECONDARY STREAM FIFO HIGHER COUNTER

Value = The number of secondary stream FIFO write strobes that occurred when the number of FIFO entries was greater than the high watermark specified in MM8204\_23-16

The counter stops incrementing when it reaches 8000H. It is reset by writing 0000H to it.

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**Secondary Stream Cb/Cr Blocks Stride Register (MM8218)**

Read/Write Address: 8218H

BCI: C6H

Power-on Default: Undefined

In YCbCr420 mode, this register defines the strides for the Cb and Cr blocks. Updating of this register is controlled via CR66\_4 and CR51\_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	SECONDARY STREAM STRIDE												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUBPICT HORIZ TILING OFFSET (QWORDS)								SUBPIC VT OFFSET				SUBPIC HT OFFSET			

## Bits 12-0 SECONDARY STREAM STRIDE

Value = byte offset of vertically adjacent pixels in the secondary stream buffer(s)

If double or triple buffering is used, the stride must be the same for all buffers.

Bits 15-13 Reserved

## Bits 19-16 SUBPICTURE HORIZONTAL TILING OFFSET

Value = Offset from horizontal tile boundary in tiles of the secondary stream subpicture

## Bits 23-20 SUBPICTURE VERTICAL TILING OFFSET

Value = Offset from vertical tile boundary in lines of the secondary stream subpicture

## Bits 31-24 SUBPICTURE HORIZONTAL TILING OFFSET (QWORDS) (Rev. B)

Value = Offset from horizontal tile boundary in QWORDS of the secondary stream subpicture

This field provides the same information (except for the units) as bits 19-16 of this register.

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**Primary Stream Frame Buffer Size Register (MM8300)**

Read/Write Address: 8300H

BCI: C7H

Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIMARY STREAM FRAME BUFFER SIZE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	SWB	EB23	PS FRAME BUFF SIZE				

## Bits 21-0 PRIMARY STREAM FRAME BUFFER SIZE

20-bit Value = # of QWords -1 allocated in the frame buffer for the primary stream

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Streams Processor Registers

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- Bit 22      EB23 - Enable Bit 23  
0 = Write blocking disabled  
1 = Enable function of bit 23 of this register (software control of write blocking)
- The power-on default value is 0. Write blocking can also be enabled via a BCI QueuedPageFlip command if this bit is cleared to 0.
- Bit 23      SWB - Software Control of Write Blocking  
0 = Write blocking disabled  
1 = Write blocking enabled
- Bit 22 of the register must be set to 1 for this to be effective. The power-on default value is 0.
- Bits 31-24    Reserved

---

**Secondary Stream Frame Buffer Size Register (MM8304)**

Read/Write                      Address: 8304H    BCI: C8H  
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY STREAM FRAME BUFFER SIZE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	SST	SS FRAME BUFF SIZE					

- Bits 21      SECONDARY STREAM FRAME BUFFER SIZE
- Value = # of QWords -1 allocated in the frame buffer for the secondary stream
- This is the size of one frame, not the total size if double or triple buffering is being used.
- Bit 22      SST - Secondary Stream Type  
0 = Secondary stream is video (YUV/YCbCr)  
1 = Secondary stream is graphics (RGB)
- Bits 31-23    Reserved

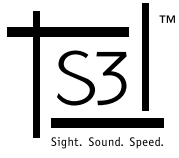
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**Secondary Stream Frame Buffer Address 2 Register (MM8308)**

Read/Write                      Address: 8308H    BCI: C9H  
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY BUFFER ADDRESS 2															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 2								

- Bits 24-0      SECONDARY BUFFER ADDRESS 2
- Value = Secondary stream frame buffer starting address 2
- This value must be quadword aligned.
- Bits 31-25    Reserved



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## Section 9: LPB/VIP Register Descriptions

LPB/VIP registers can only be accessed via memory-mapped I/O. The register identifier MMxxxx means that the register is memory mapped at offset 000 xxxxH from the base address.

### LPB Mode Register (MMFF00)

Read/Write Address: FF00H  
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDT	R	LBA	R	R	LHS	LVS	OSA	CHD	CBS	SF	LR	LPB MODE			LE
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	RIE	OEII	OEI	VI	ILC	SNO	R	VFT			R	R	R	R	R

Bit 0 LE - LPB Enable  
0 = LPB Disabled  
1 = LPB Enabled

Once enabled, the LPB is reset either by a system reset or via bit 4 of this register.

Bits 3-1 LPB MODE  
010 = Video 8 mode. 8-bit video decoder input.  
110 = VIP mode. 8-bit video or MPEG-2 decoder input.

All other values are reserved.

Bit 4 LR- LPB Reset  
0 = No effect  
1 = Reset LPB

This bit should be set and then reset before switching between LPB modes.

Bit 5 SF - Skip Frames  
0 = Write all received frames to memory  
1 = Write every other received frame to memory (1, 3, etc.)

Bit 6 CBS - Color Byte Swap  
0 = Incoming video is in Cb, Y, Cr, Y format  
1 = Incoming video is in Y, Cb, Y, Cr format

This bit does not affect VBI data.

Bit 7 CHD - Compatible Horizontal Decimation Type  
0 = Trio64+—type decimation (byte)  
1 = Trio64V2-type decimation

This bit is effective when MMFF\_15 = 0.

Bit 8 OSA - Omit Stride Add  
0 = Add stride to the end of the line  
1 = Don't add stride to the end of the line

This bit is not needed to generate contiguous video capture data in the frame buffer.

Bit 9 LVS - LPB Vertical Sync Input Polarity  
0 = LPB vertical sync input is active low  
1 = LPB vertical sync input is active high

Bit 10 LHS - LPB Horizontal Sync Input Polarity  
0 = LPB horizontal sync input is active low  
1 = LPB horizontal sync input is active high

Bits 12-11	Reserved
Bit 13	LBA - Load Base Address (Write Only)
	Writing a 1 to this bit immediately loads the base address currently being pointed to.
Bit 14	Reserved
Bit 15	HDT - Horizontal Decimation Type Select 0 = Use MMFF00_7 to select horizontal decimation type 1 = Use MMFF78_31 to select horizontal decimation type
Bits 19-16	Reserved
Bit 20	Reserved
Bits 23-21	VFT - Video FIFO Threshold 00 0= 1 FIFO slot 001 = 2 FIFO slots 010 = 4 FIFO slots 011 = 6 FIFO slots 100 = 8 FIFO slots 101 = 16 FIFO slots 110 = 24 FIFO slots 111 = 30 FIFO slots
	When this many slots are filled in the video FIFO, a request is generated to the memory manager to begin emptying the FIFO. This is used to maximize the efficiency of the memory interface. Each slot holds 2 DWords.
Bit 24	Reserved
Bit 25	SNO - Sync Non-Overlap 0 = No effect 1 = Don't add stride after first HSYNC
	This bit must be set when the first HSYNC does not occur within the VSYNC active period.
Bit 26	ILC - Invert LCLK 0 = Use LCLK as received 1 = Invert the LCLK input
Bit 27	OES - Odd/Even Detect Select 0 = Bit 28 status based on interpretation of sync signals 1 = Bit 28 status based on ODDIN pin input
Bit 28	OEI - Odd/Even Field Indicator (Read Only) 0 = Odd field being processed 1 = Even field being processed
Bit 29	OELL - Odd/Even Field Indicator Invert 0 = Odd/even field indicator as specified by bit 28 of this register 1 = Odd/even field definition is inverted from that specified by bit 28 of this register
Bit 30	RIE - Reinterlacing Enable 0 = Reinterlacing disabled 1 = Reinterlacing enabled
Bit 31	Reserved



**LPB FIFO Status Register (MMFF04)**

Read Only                      Address: FF04H

Power-on Default: 0000008H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWPS		OFAE	OFE	OFF	ORPS			OWPS			VFF	OFIFO STATUS			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	VRPS				V0A	V0E	FDM	VDD	VWPS			

- Bits 3-0      LPB Output FIFO Status  
0000 = 0 FIFO slots free  
0001 = 1 FIFO slot free  
0010 = 2 FIFO slots free  
0011 = 3 FIFO slots free  
0100 = 4 FIFO slots free  
0101 = 5 FIFO slots free  
0110 = 6 FIFO slots free  
0111 = 7 FIFO slots free  
1000 = 8 FIFO slots free  
Each slot contains 4 bytes
- Bit 4          VFF - Video FIFO Flush  
0 = No video FIFO flush  
1 = Video FIFO flush in process
- Bits 7-5      OWPS - LPB Output FIFO Write Pointer Status  
  
Value = Write pointer status
- Bits 10-8     ORPS - LPB Output FIFO Read Pointer Status  
  
Value = Read pointer status  
Bit 11          OFF - LPB Output FIFO Full  
0 = Output FIFO not full  
1 = Output FIFO full
- Bit 12        OFE - LPB Output FIFO Empty  
0 = Output FIFO not empty  
1 = Output FIFO empty
- Bit 13        OFAE - LPB Output FIFO Almost Empty  
0 = Output FIFO has something other than 1 slot filled  
1 = Output FIFO has one slot filled
- Bits 18-14    VWPS - LPB Video FIFO Write Pointer Status  
  
Value = Write pointer status
- Bit 19        VDD - VIP Device Detect  
0 = No VIP device detected at reset  
1 = VIP device detected at reset
- Bit 20        V0F - LPB Video FIFO Full  
0 = Video FIFO 0 not full  
1 = Video FIFO 0 full
- Bit 21        V0E - LPB Video FIFO Empty  
0 = Video FIFO 0 not empty  
1 = Video FIFO 0 empty
- Bit 22        V0AE - LPB Video FIFO Almost Empty  
0 = Video FIFO 0 has something other than 1 slot filled  
1 = Video FIFO 0 has one slot filled
- Bits 27-23    VRPS - LPB Video FIFO Read Pointer Status  
  
Value = Read pointer status

Bits 31-28 Reserved

**LPB Interrupt Flags Register (MMFF08)**

Read/Write Address: FF08H  
 Power-on Default: 00000000H

Note that bit 31 is read only.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	VT	R	VI	R	R	R	SPS	EFI	ELI	FEI
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VI	R	R	R	R	R	VTM	SPW	VIE	EB1E	EB0E	ODE	SPM	EFM	ELM	FEM

Bit 0 FEI - LPB Output FIFO Empty Interrupt Status  
 0 = No interrupt  
 1 = LPB output FIFO empty

Writing a 1 to this bit clears the interrupt.

Bit 1 ELI - End of Line Interrupt Status  
 0 = No interrupt  
 1 = HSYNC input received

Writing a 1 to this bit clears the interrupt.

Bit 2 EFI - End of Frame Interrupt Status  
 0 = No interrupt  
 1 = VSYNC input received

Writing a 1 to this bit clears the interrupt.

Bit 3 SPS - Serial Port Start Detect Interrupt Status  
 0 - No interrupt  
 1 = Serial port start condition detected

A serial port start condition occurs when SPD is driven low by another device while SPCLK is not being driven low. Writing a 1 to this bit clears the interrupt.

Bits 6-4 Reserved

Bit 7 VI - VBI Interrupt Status  
 0 = No interrupt  
 1 = Start of live video detected

Writing a 1 to this bit clears the interrupt.

Bit 8 Reserved

Bit 9 VT - VIP Timeout Interrupt Status  
 0 = No interrupt  
 1 = VIP timeout detected

Bits 15-10 Reserved

Bit 16 FEM - LPB Output FIFO Empty Interrupt Enable Mask  
 0 = LPB output FIFO empty interrupt disabled  
 1 = LPB output FIFO empty interrupt enabled

Bit 17 ELM - End of Line Interrupt Enable Mask  
 0 = End of Line interrupt disabled  
 1 = End of Line interrupt enabled

Bit 18 EFM - End of Frame Interrupt Enable Mask  
 0 = End of frame interrupt disabled  
 1 = End of frame interrupt enabled

LPB/VIP Registers

- Bit 19      SPM - Serial Port Start Detect Interrupt Mask  
0 = Serial port start detect interrupt disabled  
1 = Serial port start detect interrupt enabled
- Bit 20      FDM - Decimation Field Drop Interrupt Enable Mask  
0 = Decimation field drop interrupt disabled  
1 = decimation field drop interrupt enabled
- Bit 21      EB0E - Encoding Buffer 0 Interrupt Enable Mask  
0 = Encoding buffer 0 interrupt disabled  
1 = Encoding buffer 0 interrupt enabled
- Bit 22      EB1E - Encoding Buffer 1 Interrupt Enable Mask  
0 = Encoding buffer 1 interrupt disabled  
1 = Encoding buffer 1 interrupt enabled
- Bit 23      VIE - VBI Interrupt Enable Mask  
0 = VBI Interrupt disabled  
1 = VBI Interrupt enabled
- Bit 24      SPW - Serial Port Wait  
0 = Release SPCLK to float high  
1 = Drive SPCLK low upon receipt of a serial port start condition  
  
Setting this bit to 1 enables serial port wait states until the Host is ready to process the data.
- Bit 25      VTM - VIP Timeout Interrupt Mask  
0 = VIP timeout interrupt disabled  
1 = VIP timeout interrupt enabled
- Bit 30-26   Reserved
- Bit 31      VI - VSYNC Indicator (Read Only)  
0 = Active region for live video  
1 = Vertical blanking region for live video (VSYNC active)

**LPB Frame Buffer Address 0 Register (MMFF0C)**

Read/Write                      Address: FF0CH  
Power-on Default: 0000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
LPB BUFFER ADDRESS 0																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
R	R	R	R	R	R	R	LPB BUFFER ADDRESS 0										

- Bits 24-0      LPB Frame Buffer Address 0  
  
Value = starting address 0 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer  
  
If live video mirroring is enabled (MMFF00\_31 = 1), the address must be for the end of the first line. This value will normally be the same as the secondary stream frame buffer address 0. The value must start on an 8-byte boundary. A value programmed in this field does not take effect until the next LPB VSYNC.
- Bits 31-25      Reserved

---

**LPB Frame Buffer Address 1 Register (MMFF10)**

Read/Write Address: FF10H

Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
LPB BUFFER ADDRESS 1																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
R	R	R	R	R	R	R	LPB BUFFER ADDRESS 1									R	R	R	R

Bits 24-0 LPB Frame Buffer Address 1

Value = starting address 1 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer

If live video mirroring is enabled (MMFF00\_31 = 1), the address must be for the end of the first line.

This value will normally be the same as the secondary stream frame buffer address 1. Both address 0 and address 1 are defined when double buffering is used. The value must start on an 8-byte boundary. A value programmed in this field does not take effect until the next LPB VSYNC.

Bits 31-25 Reserved

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**VIP Control Register (MMFF14)**

Read/Write Address: FF14H

Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDS		VC		VIP READ/WRITE ADDRESS											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	VRR		VFW		R	R	R	R

Bits 11-0 VIP READ/WRITE ADDRESS

Value = Address of the VIP device register or FIFO to be accessed

Register addresses use bits 11-0. FIFO addresses use bits 11-8.

Bits 13-12 VC - VIP Read/Write Command

00 = Register write

01 = FIFO write

10 = Register read

11 = FIFO read (FIFO ports 0 and 1 status only)

Bits 15-14 VDS - VIP Device Select

00 = MPEG decoder

01 = Video decoder

10 = Reserved

11 = Reserved

Bits 19-16 Reserved

Bits 21-20 VFW - VIP FIFO Write Burst Length

00 = 4 bytes

01 = 8 bytes

10 = 12 bytes

11 = 16 bytes

Bits 23-22 VRR - VIP Register Read/Write Burst Length

00 = 1 byte

01 = 2 bytes

10 = 3 bytes

11 = 4 bytes (register write only)

Bits 31-24 Reserved

**VIP Read/Write Data Register (MMFF18)**

Read/Write Address: FF18H  
 Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIP READ/WRITE DATA															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIP READ/WRITE DATA															

Bits 31-0 VIP READ/WRITE DATA

A write to this register triggers a read/write sequence based on the address information in MMFF14\_11-0 for registers or 11-8 for FIFOs and the burst setting. The first byte in a burst uses bits 7-0, the second uses bits 15-8, etc.

**Serial Port 1 Register (MMFF20)**

Read/Write Address: FF20H  
 Power-on Default: 00000000H

Bits 4-0 of this register can also be accessed via CRA0\_4-0. This register is normally used for I<sup>2</sup>C communications.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	SPE	SDR	SCR	SDW	SCW
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Bit 0 SCW - Serial Clock Write  
 0 = SPCLK1 is driven low  
 1 = SPCLK1 is tri-stated  
  
 SPCLK1 carries the I2C clock. When the SPCLK1 pin is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 2 of this register.
- Bit 1 SDW - Serial Data Write  
 0 = SPD1 pin is driven low  
 1 = SPD1 pin is tri-stated  
  
 SPD1 carries the I2C data. When the SPD1 pin is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 3 of this register.
- Bit 2 SCR - Serial Clock Read (Read Only)  
 0 = SPCLK1 is low  
 1 = SPCLK1 is tri-stated (no device is driving this line)
- Bit 3 SDR - Serial Data Read (Read Only)  
 0 = SPD1 pin is low  
 1 = SPD1 pin is tri-stated (no device is driving this line)
- Bit 4 SPE - Serial Port 1 Enable  
 0 = Use of bits 1-0 of this register disabled  
 1 = Use of bits 1-0 of this register enabled
- Bits 31-5 Reserved

**LPB Video Input Window Size Register (MMFF24)**

Read/Write Address: FF24H

Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	VIDEO INPUT LINE WIDTH											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	VIDEO INPUT WINDOW HEIGHT											

Bits 11-0 VIDEO INPUT LINE WIDTH

Value = [Width in bytes of each video line] - 1

This is the width of the displayed line after the offset specified in MMFF28\_11-0. Before the 1 is subtracted in Video 8 mode, the number of pixels must be rounded up to a multiple of 2.

Bits 15-12 Reserved

Bits 27-16 VIDEO INPUT WINDOW HEIGHT

Value = [height in lines of each video input frame] - 1

This is the number of displayed lines - 1 after the offset specified in MMFF28\_24\_16.

Bits 31-28 Reserved

**LPB Video Data Offsets Register (MMFF28)**

Read/Write Address: FF28H

Power-on Default: Undefined

This register applies only to Video 8 mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	HORIZONTAL VIDEO DATA OFFSET											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	VERTICAL VIDEO DATA OFFSET											

Bits 11-0 HORIZONTAL VIDEO DATA OFFSET

Value = [number of LCLKs between HSYNC and the start of valid pixel data] - 2

Bits 15-12 Reserved

Bits 27-16 VERTICAL VIDEO DATA OFFSET

Value = number of HSYNCs between VSYNC and the first valid data line

This value must be at least 1.

Bits 31-28 Reserved

**LPB Horizontal Decimation Control Register (MMFF2C)**

Read/Write Address: FF2CH

Power-on Default: Undefined

Four different horizontal decimation schemes are provided. MMFF00\_15 = 0 means that MMFF00\_7 selects the decimation scheme. MMFF00\_15 = 1 means that MMFF78\_31 selects the decimation scheme.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO DATA MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO DATA MASK															

Bits 31-0 VIDEO DATA MASK (MMFF00\_15 = 0)

Each 32 bytes of video data input is compared with this mask. If a bit in this mask is 1, the corresponding byte is discarded. If a bit is a 0, the corresponding byte is passed to the video memory. Normally, decimation starts with bit 0 after an HSYNC. If a horizontal video data offset is specified in MMFF28\_11-0, decimation aligns with the start of data after the offset.

Bits 31-0 VIDEO DATA MASK (MMFF00\_15 = 1)

Each Y component of 32 YU or YV pairs is compared with this mask. A 0 specifies that the corresponding Y be kept and a 1 specifies that the corresponding Y be dropped. The number of 0's must be either 0 or a multiple of 4. Keep Y's are paired sequentially, with each Y pair being assigned the UV pair associated with the first Y of the pair.

**LPB Vertical Decimation Control Register (MMFF30)**

Read/Write Address: FF30H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO DATA LINE MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO DATA LINE MASK															

Bits 31-0 VIDEO DATA LINE MASK

Each 32 lines of video data input is compared with this mask. If a bit in the mask is 0, the corresponding line is passed to video memory. If a bit is a 1, the corresponding line is discarded. If a data offset is specified in MMFF28\_24-16, decimation aligns with the starting line after the offset.

**LPB Line Stride Register (MMFF34)**

Read/Write Address: FF34H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	LINE STRIDE												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 12-0 LINE STRIDE

Value = byte offset of vertically adjacent pixels

This offset is added to the line starting address each HSYNC to get the new line starting address. Each line must begin on an 8-byte boundary.

LPB/VIP Registers

Bits 31-13 Reserved

**LPB Frame Buffer Address 2 Register (MMFF38)**

Read/Write Address: FF38H  
 Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
LPB BUFFER ADDRESS 2																		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
R	R	R	R	R	R	R	LPB BUFFER ADDRESS 2											

Bits 24-0 LPB FRAME BUFFER ADDRESS 2

Value = starting address 0 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer

If live video mirroring is enabled (MMFF00\_31 = 1), the address must be for the end of the first line. This value will normally be the same as the secondary stream frame buffer address 2 and is used only for triple buffering. The value must start on an 8-byte boundary. A value programmed in this field does not take effect until the next LPB VSYNC.

Bits 31-25 Reserved

**LPB Output FIFO Register (MMFF40)**

Read/Write Address: FF40H, FF44H...FF5CH  
 Power-on Default: 00000000H

Writes to any of the addresses in this 8 doubleword address range will be transferred to the LPB output FIFO. This allows efficient use of the MOVSD assembly language instruction. Accesses must be to doubleword addresses.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUT FIFO DATA															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUT FIFO DATA															

Bits 31-0 OUTPUT FIFO DATA

Note: Software must never transfer more compressed data than there is room for in the output FIFO. This information is read from MMFF04\_3-0.

**Bilinear Decimation 1 Register (MMFF70)**

Read/Write Address: FF70H  
 Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DESTINATION WIDTH				SOURCE WINDOW WIDTH														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
R	R	R	R	R	R	R	R	DESTINATION WINDOW WIDTH										

Bits 11-0 SOURCE WINDOW WIDTH

Value = Source window width in pixels (Ws)



Bits 23-12 DESTINATION WINDOW WIDTH  
 Value = Destination window width in pixels (Wd)

Bits 31-24 Reserved

**LPB Bilinear Decimation 2 Register (MMFF74)**

Read/Write Address: FF74H  
 Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
INTEGER FACTOR				DECIMAL DECIMATION FACTOR													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
R	R	R	R	R	R	R	R	INTEGER DECIMATION FACTOR									

Bits 11-0 DECIMAL DECIMATION FACTOR  
 Value = Decimal value of Ws/Wd (bilinear)  
 Value = Decimal value of (Ws/Wd)/2 (quadlinear)

See MMFF70 for the definitions of Ws and Wd. For example, if Ws = 640 and Wd = 260, Ws/Wd = 2.461538461538. The integer value (2) is programmed in bits 23-12 and the decimal value (461538461538) is programmed in bits 11-0.

Bits 23-12 INTEGER DECIMATION FACTOR  
 Value = Integer value of Ws/Wd

Bits 31-24 Reserved

**LPB Bilinear Decimation 3 Register (MMFF78)**

Read/Write Address: FF78H  
 Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
OFFSET INTEGER = 0				OFFSET DECIMAL VALUE													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
QDE	R	R	R	R	R	R	R	OFFSET INTEGER VALUE = 0									

Bits 11-0 OFFSET DECIMAL VALUE  
 Value = Decimal value of the offset for starting the line decimation

The offset value must be less than or equal to 0.5. This can be used to improve the selection of pixels for decimation.

Bits 23-12 OFFSET INTEGER VALUE  
 Value = Integer value of the offset for starting the line decimation  
 This value must be all 0's.

Bits 30-24 Reserved

Bit 31 QDE - Quadlinear Decimation Enable  
 0 = Disable quadlinear decimation  
 1 = Enable quadlinear decimation

---

**VBI Select Register (MMFF8C)**

Read/Write Address: FF8CH

Power-on Default: 00000000H

Only bit 1 of this register is required (and effective) when sliced VBI data is being captured (FFA0\_4 = 1).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBI WIDTH										VBI HEIGHT					VE
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	VBI STRIDE													WIDTH	

Bit 0 VE - VBI Enable  
0 = VBI data capture disabled  
1 = VBI data capture enabled

Bits 5-1 VBI Height  
Value = # of data lines to be captured in VBI period

Bits 17-6 VBI Width  
Value = [# of bytes in a VBI line] - 1 (8-bit input)  
Value = [# of words in a VBI line] - 1 (16-bit input)  
This value includes only valid data after the horizontal offset specified in MMFF94\_11-0)

Bits 30-18 VBI Stride  
Value = QWord-aligned byte offset of vertically adjacent pixels  
This must be the same as the line width for contiguous data.

Bit 31 Reserved

---

**VBI Base Address Register (MMFF90)**

Read/Write Address: FF90H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
VBI BASE ADDRESS																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
R	R	R	R	R	R	R	VBI BASE ADDRESS										

Bits 24-0 VBI Base Address  
Value = Starting address for writing VBI data to the frame buffer  
The address must be quadword aligned.

Bits 31-25 Reserved

---

**VBI Data Offset Register (MMFF94)**

Read/Write Address: FF94H

Power-on Default: 00000000H

This register is not effective is sliced VBI data is being captured (MMFFA0\_4 = 1).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	VBI HORIZONTAL DATA OFFSET											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	VBI VERTICAL DATA OFFSET								

Bits 11-0 VBI Horizontal Data Offset

Value = # of character clocks from HSYNC active and the start of valid VBI data

Bits 15-12 Reserved

Bits 24-16 VBI Vertical Data Offset

Value = # of HSYNCs between VSYNC active and the first valid VBI line

Bits 31-25 Reserved

---

**VBI Vertical Decimation Control Register (MMFF98)**

Read/Write Address: FF98H

Power-on Default: 00000000H

This register is not effective is sliced VBI data is being captured (MMFFA0\_4 = 1).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBI DATA LINE MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VBI DATA LINE MASK															

Bits 31-0 VBI Data Line Mask

If a bit in the mask is 0, the corresponding line is passed to video memory. If a bit is a 1, the corresponding line is discarded.

Bit 31 aligns with the first VBI line to be captured as defined by the vertical data offset.

**VBI Control Register (MMFF9C)**

Read/Write Address: FF9CH

Power-on Default: 0000000H

This register is not effective is sliced VBI data is being captured (MMFFA0\_4 = 1).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	FFE	DSE	PWE	R	R	VBLANK WIDTH					PV
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Bit 0 Pseudo VBLANK  
0 = Do not create and use pseudo VBLANK signal  
1 = Create and use pseudo VBLANK signal
- This feature is used to provide a vertical blanking signal when one is not provided by the digitizer. When VSYNC is received, VBLANK goes high and stays high for the number of HSYNCs programmed in bits 5-1. When this bit is set, VBI data is captured during the VBLANK period.
- Bits 5-1 VBLANK Width
- Value = Width of VBLANK signal in HSYNCs
- Bits 7-6 Reserved
- Bit 8 PWE - Partial Write Enable  
0 = Disable partial write of VBI data (less than DWord)  
1 = Enable partial write of VBI data (less than DWord)
- Setting this bit enables capture of VBI data lines that do not end on a DWord boundary.
- Bit 9 DSE - VBI Data Byte Swap Enable  
0 = Disable byte swap of VBI data  
1 = Enable byte swap of VBI data
- When this bit is enabled, the bytes in each DWord are swapped.
- Bit 10 FFE - Video FIFO Flush Enable  
0 = Disable video FIFO flushing at the end of the VBI line  
1 = Enable video FIFO flushing at the end of the VBI line
- When this bit is enabled, the video FIFO is flushed at the end of the VBI line or upon receipt of HSYNC, whichever comes first.
- Bit 31-11 Reserved

**VIP Transfer Control Register (MMFFA0)**

Read/Write Address: FFA0H

Power-on Default: 000000FH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	S/2	R	R	TB	PDS	R	VDT	VIP TIMEOUT			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 3-0 VIP TIMEOUT

Value = # of VIP phases

An interrupt can be generated based on this timeout. See MMFF08\_8. The power-on default is 1111b.

Bit 4 VDT - VBI Data Type

0 = Capture raw VBI data (required for Video 8 mode)

1 = Capture sliced VBI data

Bit 5 Reserved

Bit 6 PDS - Slave Power Down Signal

0 = VIP slave device power up signal (VIPCLK running)

1 = VIP slave device power down signal (VIPCLK turned off)

Setting this bit stops VIPCLK when the next idle state is reached.

Bit 7 TB - Task Bit

0 = Task bit = 0 for active video

1 = Task bit = 1 for active video

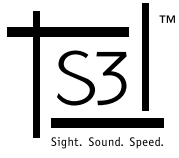
Bits 9-8 Reserved

Bit 10 S/2 - Divide SCLK By 2

0 = SCLK undivided

1 = Divide SCLK by 2 for VIPCLK

Bits 31-11 Reserved



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## Section 10: 3D Engine Register Descriptions

All 3D engine registers described below are normally accessed via the BCI. However, they can be directly accessed via memory-mapped I/O. The register identifier MM4xxx means that the register is memory mapped at offset 004 xxx from the base address. Registers/bits marked "Global" affect all triangle drawing operations and therefore should be reprogrammed only when the command queue is empty and the 3D engine is idle. Registers/bits marked "Local" can be changed on a triangle by triangle basis without affecting previously specified triangles.

---

### Vertex 0 Z Coordinate Register (MM48508) (Rev. B)

Read/Write Address: 104 8508H  
 Power-on Default: 00000000H

BCI: 02H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTEX 0 Z COORDINATE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTEX 0 Z COORDINATE															

Bits 31-0 VERTEX 0 Z COORDINATE

Value = z coordinate expressed in IEEE single precision floating point format

---

### Vertex 1 Z Coordinate Register (MM48528) (Rev B)

Read/Write Address: 104 8528H  
 Power-on Default: 00000000H

BCI: 0AH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTEX 1 Z COORDINATE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTEX 1 Z COORDINATE															

Bits 31-0 VERTEX 0 Z COORDINATE

Value = z coordinate expressed in IEEE single precision floating point format

---

### Vertex 2 Z Coordinate Register (MM48548) (Rev. B)

Read/Write Address: 104 8548H  
 Power-on Default: 00000000H

BCI: 12H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTEX 2 Z COORDINATE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTEX 2 Z COORDINATE															

Bits 31-0 VERTEX 2 Z COORDINATE

Value = z coordinate expressed in IEEE single precision floating point format

**Z Pixel Offset Register (MM48580) (Rev. A only – Removed from Rev. B)**

Read/Write Address: 004 8580H

BCI:1DH

Power-On Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z PIXEL OFFSET												R	R	R	R
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Z PIXEL OFFSET															

Bits 3-0 Reserved

Bits 31-4 Z PIXEL OFFSET

Value = z pixel offset in 1.8.19 (float)

Flush the front end when this value is changed.

**Draw Local Control Register (MM48584)**

Read/Write Address: 004 8584H

BCI:1EH

Power-On Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	BFA	SABM		D-S		DABM		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FZ	FW	SS	SM	ZE	DE	FZ	R	R	R	R	R	R	R	R	R

Bits 2-0 DABM - Destination Alpha Blend Mode

- 000 = Zero
- 001 = One
- 010 = Source color
- 011 = 1 - source color
- 100 = Source alpha
- 101 = 1 - source alpha
- 110 = Destination alpha
- 111 = 1 - destination alpha

Bit 3 D-S - Destination Color - Source Color

- 0 = Disable
- 1 = Enable this alpha blending mode (other alpha blending modes are disabled)

Bits 6-4 SABM - Source Alpha Blend Mode

- 000 = Zero
- 001 = One
- 010 = Destination color
- 011 = 1 - destination color
- 100 = Source alpha
- 101 = 1 - source alpha
- 110 = Destination alpha
- 111 = 1 - destination alpha

Bit 7 BFA - Binary Final Alpha

- 0 = Alpha for alpha blending source can be any value between 0-255
- 1 = Alpha for alpha blending source must be either 0 or 255

Bits 24-8 Reserved



3D Engine Registers

- Bit 25      FZ - Force Z Writes Till After Alpha Test  
 0 = Do Z reads and writes before texture reads  
 1 = Do Z writes after alpha test  
  
 Setting this bit to 1 may require flushing the pixel pipeline between triangles.
- Bit 26      DE - Draw Update Enable  
 0 = Draw update disabled  
 1 = Draw update enabled
- Bit 27      ZE - Z Update Enable  
 0 = Z update disabled  
 1 = Z update enabled
- Bit 28      SM - Shade Mode  
 0 = Gouraud  
 1 = Flat (vertex 2 colors)
- Bit 29      SS - Specular Shading Enable  
 0 = Specular shading disabled  
 1 = Specular shading enabled
- Bit 30      FW - Flush Pending Destination Writes  
 0 = Do not flush pending destination writes  
 1 = Flush pending destination writes before doing destination reads for this triangle  
  
 If this bit is set, the destination write low watermark (MM485EC\_17-12) must be programmed to all 0's and MM85EC\_31-30 must be programmed to 01b.
- Bit 31      FZ - Flush Pending Z Writes  
 1 = Do not flush pending Z writes  
 1 = Flush pending Z writes before doing Z reads for this triangle  
  
 If this bit is set, the Z write low watermark (MM485E8\_21-16) must be programmed to all 0's.

**Texture Palette Address Register (MM48588) (Local)**

Read/Write                      Address: 004 8588H    BCI: 1FH  
 Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PALETTE DATA ADDRESS													R	R	R
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PALETTE DATA ADDRESS															

- Bits 2-0      Reserved
- Bits 31-3    PALETTE DATA ADDRESS  
  
 Value = QWord-aligned address in memory of the texture palette  
  
 This must be a linear address in AGP memory. For frame buffer memory, only bits 25-3 are valid.

---

**Texture 0 Control Register (MM4858C) (Local)**

Read/Write Address: 004 858CH

BCI: 20H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX D LEVEL				MIPMAP LEVEL BIAS								EM	FILT MODE		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A2I	A1I	ABAS		C2I	C1I	CA2	CA1	CBAS		ETT	CC	TVAM		TUAM	

- Bits 1-0 FILTER MODE  
00 = Point sample (1TPP)  
01 = Bilinear (4TPP)  
10 = Reserved  
11 = Trilinear (16TPP)
- Bit 2 Enable MIPmapping  
0 = Treat texture as a single map level (if MIPmapped, use level 0 only)  
1 = Enable MIPmapping
- Bits 11-3 MIPMAP LEVEL BIAS  
Value = Constant offset to MIPmap level (S4.4)
- Bits 15-12 MAX D LEVEL  
Value = Maximum D level
- Bits 17-16 TUAM - Texture U Address Mode  
00 = Wrap  
01 = Clamp  
10 = Mirror  
11 = Reserved
- Bits 19-18 TVAM - Texture V Address Mode  
00 = Wrap  
01 = Clamp  
10 = Mirror  
11 = Reserved
- Bit 20 CC - Color Compare Enable  
0 = Disabled  
1 = Enabled
- Bit 21 ETT - Enable Texture Transparency  
0 = Disable texture transparency  
1 = Enable texture transparency
- Bits 23-22 CBAS - Color Blend Alpha Select  
00 = TEXTURE ALPHA  
01 = DIFFUSE ALPHA  
10 = FACTOR ALPHA  
11 = CURRENT ALPHA
- Bit 24 CA1 - Color Arg1 Copy Alpha Enable  
0 = Disabled  
1 = Enabled
- Bit 25 CA2 - Color Arg2 Copy Alpha Enable  
0 = Disabled  
1 = Enabled
- Bit 26 C1I- Color Arg1 Invert Enable  
0 = Disable  
1 = Enable

- Bit 27 C2I - Color Arg2 Invert Enable  
0 = Disable  
1 = Enable
- Bits 29-28 ABAS - Alpha Blend Alpha Select  
00 = TEXTURE ALPHA  
01 = DIFFUSE ALPHA  
10 = FACTOR ALPHA  
11 = CURRENT ALPHA
- Bit 30 A1I - Alpha Arg1 Invert Enable  
0 = Disable  
1 = Enable
- Bit 31 A2I - Alpha Arg2 Invert Enable  
0 = Disable  
1 = Enable

**Texture 1 Control Register (MM48590) (Local)**

Read/Write Address: 004 8590H  
Power-on Default: 00000000H

BCI: 21H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX D LEVEL				MIPMAP LEVEL BIAS								EM	FILT MODE		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A2I	A1I	ABAS		C2I	C1I	CA2	CA1	CBAS	ETT	CC	TVAM		TUAM		

- Bits 1-0 FILTER MODE  
00 = Point sample (1TPP)  
01 = Bilinear (4TPP)  
10 = Reserved  
11 = Trilinear (16TPP)
- Bit 2 Enable MIPmapping  
0 = Treat texture as a single map level (if MIPmapped, use level 0 only)  
1 = Enable MIPmapping
- Bits 11-3 MIPMAP LEVEL BIAS  
  
Value = Constant offset to MIPmap level (S4.4)
- Bits 15-12 MAX D LEVEL  
  
Value = Maximum D level
- Bits 17-16 TUAM - Texture U Address Mode  
00 = Wrap  
01 = Clamp  
10 = Mirror  
11 = Reserved
- Bits 19-18 TVAM - Texture V Address Mode  
00 = Wrap  
01 = Clamp  
10 = Mirror  
11 = Reserved
- Bit 20 CC - Color Compare Enable  
0 = Disabled  
1 = Enabled
- Bit 21 ETT - Enable Texture Transparency  
0 = Disable texture transparency  
1 = Enable texture transparency

---

3D Engine Registers

- Bits 23-22    CBAS - Color Blend Alpha Select  
               00 = TEXTURE ALPHA  
               01 = DIFFUSE ALPHA  
               10 = FACTOR ALPHA  
               11 = CURRENT ALPHA
- Bit 24        CA1 - Color Arg1 Copy Alpha Enable  
               0 = Disabled  
               1 = Enabled
- Bit 25        CA2 - Color Arg2 Copy Alpha Enable  
               0 = Disabled  
               1 = Enabled
- Bit 26        C1I- Color Arg1 Invert Enable  
               0 = Disable  
               1 = Enable
- Bit 27        C2I- Color Arg2 Invert Enable  
               0 = Disable  
               1 = Enable
- Bits 29-28    ABAS - Alpha Blend Alpha Select  
               00 = TEXTURE ALPHA  
               01 = DIFFUSE ALPHA  
               10 = FACTOR ALPHA  
               11 = CURRENT ALPHA
- Bit 30        A1I - Alpha Arg1 Invert Enable  
               0 = Disable  
               1 = Enable
- Bit 31        A2I - Alpha Arg2 Invert Enable  
               0 = Disable  
               1 = Enable

---

**Texture 0 Address Register (MM48594) (Local)**

Read/Write                      Address: 004 8594H  
 Power-on Default: 00000000H

BCI: 22H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEXTURE DATA ADDRESS													R	R=1	TL
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEXTURE DATA ADDRESS															

- Bit 0        TL - Texture Location  
               0 = Texture is in frame buffer memory  
               1 = Texture is in AGP memory

Bit 1        Reserved = 1

This bit must always be set to 1 when texture 0 is used.

Bit 2        Reserved

Bits 31-3    TEXTURE DATA ADDRESS

Value = QWord-aligned address in memory of the texture palette

This must be a linear address in system memory. For frame buffer memory, only bits 24-3 are valid.

**Texture 1 Address Register (MM48598) (Local)**

Read/Write Address: 004 8594H

BCI: 23H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEXTURE DATA ADDRESS													R	R=1	TL
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEXTURE DATA ADDRESS															

Bit 0 TL - Texture Location  
 0 = Texture is in frame buffer memory  
 1 = Texture is in AGP memory

Bit 1 Reserved = 1

This bit must always be set to 1 when texture 1 is used.

Bit 2 Reserved

Bits 31-3 TEXTURE DATA ADDRESS

Value = QWord-aligned address in memory of the texture palette

This must be a linear address in system memory. For frame buffer memory, only bits 24-3 are valid.

**Texture 0 Blending Control Register (MM4859C) (Local)**

Read/Write Address: 004 859CH

24H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAB	CD2	CDB	CAS		CM2		CM1	CPS	CI2	C1A	CA2		CA1		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLS		CDM	ASC	CSC	AD2	ADB	AAS	AM2		AM1	AA2		AA1		

Bits 1-0 CA1 - Color Argument 1 Select  
 00 = TA\_TEXTURE  
 01 = TA\_DIFFUSE  
 10 = TA\_FACTOR  
 11 = TA\_CURRENT

Bits 4-2 CA2 - Color Argument 2 Select  
 000 = TA\_CURRENT  
 001 = TA\_DIFFUSE  
 010 = TA\_FACTOR  
 011 = TA\_SPECULAR  
 100 = TA\_TEXTURE

All other values are reserved.

Bit 5 CIA - Color Invert Alpha Enable  
 0 = Disabled  
 1 = Enabled

Bit 6 CI2 - Color Invert Arg2 Enable for Mod1  
 0 = Disabled  
 1 = Enabled

Bit 7 CPS - Color Pre-Modulate Select  
 0 = Select Arg1 input color  
 1 = Select Arg1 input alpha

Bit 8	CM1 - Color Mod1 Select 0 = Select Arg1 1 = Select zero
Bits 10-9	CM2 - Color Mod2 Select 00 = Select Arg2 01 = Select Alpha 10 = Select 255 11 = Select premod
Bits 12-11	CAS - Color Add Select 00 = Select zero 01 = Select Arg2 10 = Reserved 11 = Select Alpha
Bit 13	CDB - Color Do Blend 0 = No blending 1 = Do blend
Bit 14	CD2 - Color Do 2's Complement 0 = No 2's complement 1 = Do 2's complement
Bit 15	CAB - Color Add Bias -0.5 Enable 0 = Disable 1 = Enable
Bits 17-16	AA1 - Alpha Argument 1 Select 00 = TA_TEXTURE 01 = TA_DIFFUSE 10 = TA_FACTOR 11 = TA_CURRENT
Bits 20-18	AA2 - Alpha Argument 2 Select 000 = TA_CURRENT 001 = TA_DIFFUSE 010 = TA_FACTOR 011 = TA_SPECULAR 100 = TA_TEXTURE
	All other values are reserved.
Bit 21	AM1 - Alpha Mod1 Select 0 = Select Arg1 1 = Select zero
Bits 23-22	AM2 - Alpha Mod2 Select 00 = Select Arg2 01 = Select Alpha 10 = Select 255 11 = Select premod
Bit 24	AAS Alpha Add Select 0 = Select zero 1 = Select Arg2
Bit 25	ADB - Alpha Do Blend 0 = No blending 1 = Do blend
Bit 26	AD2 - Alpha Do 2's Complement 0 = No 2's complement 1 = Do 2's complement
Bit 27	CSC - Color Stage Clamping Enable 0 = Disable 1 = Enable

- Bit 28      ASC - Alpha Stage Clamping Enable  
0 = Disable  
1 = Enable
- Bit 29      CDM - Color Do Diffuse Mul  
0 = No diffuse mul  
1 = Do diffuse mul
- Bits 31-30    CLS - Color Left Shift  
00 = No shift  
01 = 2x shift  
10 = 4x shift  
11 = Reserved

**Texture 1 Blending Control Register (MM485A0) (Local)**

Read/Write

Address: 004 85A0H

25H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAB	CD2	CDB	CAS		CM2		CM1	CPS	CI2	C1A	CA2		CA1		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLS		R	ASC	CSC	AD2	ADB	AAS	AM2		AM1	AA2		AA1		

- Bits 1-0      CA1 - Color Argument 1 Select  
00 = TA\_TEXTURE  
01 = TA\_DIFFUSE  
10 = TA\_FACTOR  
11 = TA\_CURRENT
- Bits 4-2      CA2 - Color Argument 2 Select  
000 = TA\_CURRENT  
001 = TA\_DIFFUSE  
010 = TA\_FACTOR  
011 = TA\_SPECULAR  
100 = TA\_TEXTURE
- All other values are reserved.
- Bit 5          CIA - Color Invert Alpha Enable  
0 = Disabled  
1 = Enabled
- Bit 6          CI2 - Color Invert Arg2 Enable for Mod1  
0 = Disabled  
1 = Enabled
- Bit 7          CPS - Color Pre-Modulate Select  
0 = Select Arg1 input color  
1 = Select Arg1 input alpha
- Bit 8          CM1 - Color Mod1 Select  
0 = Select Arg1  
1 = Select zero
- Bits 10-9      CM2 - Color Mod2 Select  
00 = Select Arg2  
01 = Select Alpha  
10 = Select 255  
11 = Select premod
- Bits 12-11    CAS - Color Add Select  
00 = Select zero  
01 = Select Arg2  
10 = Reserved  
11 = Select Alpha

Bit 13	CDB - Color Do Blend 0 = No blending 1 = Do blend
Bit 14	CD2 - Color Do 2's Complement 0 = No 2's complement 1 = Do 2's complement
Bit 15	CAB - Color Add Bias -0.5 Enable 0 = Disable 1 = Enable
Bits 17-16	AA1 - Alpha Argument 1 Select 00 = TA_TEXTURE 01 = TA_DIFFUSE 10 = TA_FACTOR 11 = TA_CURRENT
Bits 20-18	AA2 - Alpha Argument 2 Select 000 = TA_CURRENT 001 = TA_DIFFUSE 010 = TA_FACTOR 011 = TA_SPECULAR 100 = TA_TEXTURE
	All other values are reserved.
Bit 21	AM1 - Alpha Mod1 Select 0 = Select Arg1 1 = Select zero
Bits 23-22	AM2 - Alpha Mod2 Select 00 = Select Arg2 01 = Select Alpha 10 = Select 255 11 = Select premod
Bit 24	AAS Alpha Add Select 0 = Select zero 1 = Select Arg2
Bit 25	ADB - Alpha Do Blend 0 = No blending 1 = Do blend
Bit 26	AD2 - Alpha Do 2's Complement 0 = No 2's complement 1 = Do 2's complement
Bit 27	CSC - Color Stage Clamping Enable 0 = Disable 1 = Enable
Bit 28	ASC - Alpha Stage Clamping Enable 0 = Disable 1 = Enable
Bit 29	Reserved
Bits 31-30	ALS - Alpha Left Shift 00 = No shift 01 = 2x shift 10 = 4x shift 11 = Reserved



**Texture Transparent Color Register (MM485A4) (Local)**

Read/Write Address: 004 85A4H

BCI: 26H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRANSPARENT TEXTURE COLOR 0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRANSPARENT TEXTURE COLOR 1															

Bits 15-0 TRANSPARENT TEXTURE COLOR 0

Value = RGB565 (if ARGB1555 or ARGB4444 texture convert color to RGB565)  
Value = CLUT1555 or CLUT4444 (8-bit palettized mode)

Each texel color value read from memory is compared with this value. If it matches, the texel is considered to be fully transparent (alpha = 00H). For non-matches, the texel is considered to be opaque (alpha = FFH). This function is not supported in other modes. The compare enable is MM4858C\_21.

Bits 31-16 TRANSPARENT TEXTURE COLOR 1

See the description for bits 15-0. The compare enable is MM48590\_21.

**Texture Description Register (MM485A8) (Local)**

Read/Write Address: 004 85A8H

BCI: 27H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
TEXTURE 1 WIDTH				TEXTURE 0 FORMAT				TEXTURE 0 HEIGHT				TEXTURE 0 WIDTH					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
LTP		TPS		DF		PD		T1		T0		TBL		TEXTURE 1 FORMAT		TEXTURE 1 HEIGHT	

Bits 3-0 TEXTURE 0 WIDTH

Value = n

where the texture width is 2\*\*n. The maximum n allowed is 11 (width = 2048)

Bits 7-4 TEXTURE 0 HEIGHT

Value = n

where the texture height is 2\*\*n. The maximum n allowed is 11 (height = 2048)

Bits 11-8 TEXTURE 0 FORMAT  
0000 = 4 bits/texel S3TC (block truncation coded)  
0001 = 8 bits/texel color index. Palette entry format is RGB565. Palette table required.  
0010 = 8 bits/texel color index. Palette entry format is ARGB1555. Palette table required.  
0011 = 32 bits/texel ARGB8888  
0100 = 16 bits/texel ARGB1555  
0101 = 16 bits/texel ARGB4444  
0110 = 16 bits/texel RGB565  
0111 = 8 bits/texel color index. Palette entry format is ARGB4444. Palette table required.  
1000 = 8-bit S3TC format with 4-bit alpha followed by 4-bit S3TC color  
1001 = 8-bit S3TC format with 4-bit S3TC alpha followed by 4-bit S3TC color  
1010 = 4-bit S3TC format without alpha - L4, duplicate color, put alpha = FFH  
1011 = 8-bit S3TC format with 4-bit alpha - A4L4, duplicate color  
1100 = Luminance texture - L8, duplicate color, put alpha = FFH  
1101 = Luminance alpha texture - A4L4, duplicate color and alpha  
1110 = Intensity texture - L8, duplicate color and alpha  
1111 = Alpha texture - A8, all colors set to FFH except alpha

Bits 15-12 TEXTURE 1 WIDTH

Value = n

where the texture width is  $2^{*}n$ . The maximum n allowed is 11 (width = 2048)

Bits 19-16 TEXTURE 1 HEIGHT

Value = n

where the texture height is  $2^{*}n$ . The maximum n allowed is 11 (height = 2048)

Bits 23-20 TEXTURE 1 FORMAT

0000 = 4 bits/texel S3TC (block truncation coded)  
0001 = 8 bits/texel color index. Palette entry format is RGB565. Palette table required.  
0010 = 8 bits/texel color index. Palette entry format is ARGB1555. Palette table required.  
0011 = 32 bits/texel ARGB8888  
0100 = 16 bits/texel ARGB1555  
0101 = 16 bits/texel ARGB4444  
0110 = 16 bits/texel RGB565  
0111 = 8 bits/texel color index. Palette entry format is ARGB4444. Palette table required.  
1000 = 8-bit S3TC format with 4-bit alpha followed by 4-bit S3TC color  
1001 = 8-bit S3TC format with 4-bit S3TC alpha followed by 4-bit S3TC color  
1010 = 4-bit S3TC format without alpha - L4, duplicate color, put alpha = FFH  
1011 = 8-bit S3TC format with 4-bit alpha - A4L4, duplicate color  
1100 = Luminance texture - L8, duplicate color, put alpha = FFH  
1101 = Luminance alpha texture - A4L4, duplicate color and alpha  
1110 = Intensity texture - L8, duplicate color and alpha  
1111 = Alpha texture - A8, all colors set to FFH except alpha

Bit 24 TBL - Texture Blending Loop Enable

0 = Disabled  
1 = Enabled

Bit 25 T0 - Texture 0 Enable

0 = Disabled  
1 = Enabled

Bit 26 T1 - Texture 1 Enable

0 = Disabled  
1 = Enabled

3D Engine Registers

Bit 27 PD - Perspective Correction Disable  
 0 = Enabled  
 1 = Disabled

Setting this bit disables perspective correction by forcing the W value used by the hardware to always be 1. This bit is reserved in Rev. B (no disable for perspective correction).

Bit 28 DF - Use D Fraction for Alpha  
 0 = Disabled  
 1 = Enabled

MipMapping must be enabled before this is enabled.

Bits 30-29 TPS - Texture Palette Size  
 00 = 64 entries (16 QWords)  
 01 = 128 entries (32 QWords)  
 10 = 192 entries (48 QWords)  
 11 = 256 entries (64 QWords)

Bit 31 LTP - Load Texture Palette  
 0 = No effect  
 1 = Load new texture palette

**Fog Table 0-7 Registers (MM485AC - MM485C8) (Global)**

Read/Write Address: See below.  
 Power-on Default: 00000000H

There are 8 Fog Table registers, each with the same definition given below. The register addresses are:

Fog Table Register # (n)	MMIO Address (Hex)	BCI Address (Hex)
0 (Entries 0-3)	004 85AC	28
1 (Entries 4-7)	004 85B0	29
2 (Entries 8-11)	004 85B4	2A
3 (Entries 12-15)	004 85B8	2B
4 (Entries 16-19)	004 85BC	2C
5 (Entries 20-23)	004 85C0	2D
6 (Entries 24-27)	004 85C4	2E
7 (Entries 28-31)	004 85C8	2F

The definition for each is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOG VALUE 4n+1								FOG VALUE 4n							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOG VALUE 4n+3								FOG VALUE 4n+2							

Bits 7-0 FOG VALUE 4n  
 Value = 8-bit fog value 4n computed from fog parameters

n = Fog table register number

Bits 15-8 FOG VALUE 4n+1  
 Value = 8-bit fog value 4n+1 computed from fog parameters

n = Fog table register number

- Bits 23-16 FOG VALUE 4n+2  
 Value = 8-bit fog value 4n+2 computed from fog parameters  
 n = Fog table register number
- Bits 31-24 FOG VALUE 4n+3  
 Value = 8-bit fog value 4n+3 computed from fog parameters  
 n = Fog table register number

**Fog Control Register (MM485CC) (Global)**

Read/Write Address: 004 85CCH  
 Power-on Default: 00000000H

BCI: 30H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN FOG COLOR								BLUE FOG COLOR							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END SHIFT		FM	FE	R	TOTAL SHIFT			RED FOG COLOR							

- Bits 7-0 BLUE FOG COLOR  
 Value = Blue fog color
- Bits 15-8 GREEN FOG COLOR  
 Value = Green fog color
- Bits 23-16 RED FOG COLOR  
 Value = Red fog color
- Bit 26-24 TOTAL SHIFT - Fog Table Z Total Shift  
 Value = Total bit length of shared pattern of Zw
- Bit 27 Reserved
- Bit 28 FE - Fog Enable  
 0 = Disable fog  
 1 = Enable fog
- Bit 29 FM - Fog Mode  
 0 = Use table fog  
 1 = Use vertex fog parameter
- Bit 31-30 END SHIFT - Fog Table Z End Shift  
 Value = Number of 0's in the shared Zw pattern (max 3)

**Stencil Control Register (MM485D0) (Global)**

Read/Write Address: 004 85D0H

BCI: 31H

Power-on Default: 00000000H

To use the stencil function, alpha testing must be disabled (MM485E4\_31 = 0) and a 24-bit Z-Buffer must be defined and enabled (MM485D8\_5 and 31 = 1). The stencil reference value (Sref below) is defined in MM485D8\_23-16. The stencil frame buffer value is stored in the upper 8 bits of the 32-bit Z value that is used when 24-bit Z-Buffering is specified.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
STENCIL WRITE MASK				STENCIL READ MASK								SE	ST COMPARE			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	R	R	ST PASS/Z PASS			ST PASS/Z FAIL			STENCIL FAIL			STENCIL WRITE MASK				

Bits 2-0 ST COMPARE - Stencil Compare Mode  
 000 = Never passes  
 001 = Pass if Sref < Sfb  
 010 = Pass if Sref = Sfb  
 011 = Pass if Sref ≤ Sfb  
 100 = Pass if Sref > Sfb  
 101 = Pass if Sref ≠ Sfb  
 110 = Pass if Sref ≥ Sfb  
 111 = Always passes

Bit 3 SE - Stencil Enable  
 0 = Disable  
 1 = Enable

Bits 11-4 STENCIL READ MASK

Bit positions set to 1 will be read.

Bits 19-12 STENCIL WRITE MASK

Bit positions set to 1 will be written.

Bits 22-20 STENCIL FAIL  
 000 = Sfb = Sfb  
 001 = Sfb = 0  
 010 = Sfb = Sref  
 011 = Sfb++ Clamp (increment and clamp)  
 100 = Sfb- Clamp (decrement and clamp)  
 101 = Sfb = ^Sfb (invert)  
 110 = Sfb++ (increment)  
 111 = Sfb- (decrement)

Bits 25-23 STENCIL PASS/Z FAIL  
 000 = Sfb = Sfb  
 001 = Sfb = 0  
 010 = Sfb = Sref  
 011 = Sfb++ Clamp (increment and clamp)  
 100 = Sfb- Clamp (decrement and clamp)  
 101 = Sfb++ (increment)  
 110 = Sfb- (decrement)  
 111 = Sfb = ^Sfb (invert)

Bits 28-26 STENCIL PASS/Z PASS  
 000 = Sfb = Sfb  
 001 = Sfb = 0  
 010 = Sfb = Sref  
 011 = Sfb++ Clamp (increment and clamp)  
 100 = Sfb- Clamp (decrement and clamp)  
 101 = Sfb = ^Sfb (invert)  
 110 = Sfb++ (increment)  
 111 = Sfb- (decrement)

Bits 31-29 Reserved

---

**Z-Buffer Control Register (MM485D4) (Global)**

Read/Write Address: 004 85D4H  
 Power-on Default: 00000000H

BCI: 32H

In the normal case for Rev. A, the W values from the vertex data are used in conjunction with this buffer. Therefore, "W" should replace "Z" in most instances below. The term Z-Buffer is retained here because this is the buffer that is used for the function that is normally associated with the term Z-Buffer, i.e., depth testing.

For Rev. B, both W buffering and true Z buffering are available (see bit 31).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	Z EXPONENT OFFSET								R	EZ	R	R	ZB COMP			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
ZID	FZ	R	R	R	R	FID	AZ	STENCIL REFERENCE VALUE								

Bits 2-0 ZB COMP - Z-Buffer Compare Mode  
 000 = z compare never passes  
 001 = Pass if Znew < Zzb  
 010 = Pass if Znew = Zzb  
 011 = Pass if Znew ≤ Zzb  
 100 = Pass if Znew > Zzb  
 101 = Pass if Znew ≠ Zzb  
 110 = Pass if Znew ≥ Zzb  
 111 = z compare always passes

Bits 4-3 Reserved

Bit 5 EZ - Enable Z-Buffer  
 0 = Disable Z compare and Z-Buffer updates  
 1 = Enable Z compare and Z-Buffer updates

Bit 6 Reserved

Bits 14-7 Z EXPONENT OFFSET  
 Value = 8-bit 2's complement Z exponent offset

This value is used to adjust the Z (actually W) range so that a fixed Z format can be used. The adjusted Z is then inverted and stored in the Z-Buffer unless bit 31 of this register is set to 1.

Bit 15 Reserved

Bits 23-16 STENCIL REFERENCE VALUE  
 Value - Sref value to be used in stencil comparisons (see MM485D0)

Bit 24 AZ - Auto Z Clear Enable  
 0 = Auto Z clear disabled  
 1 = Auto Z clear enabled

Bit 25 FID - Frame ID  
 When auto Z clear is enabled via bit 24 of this register, the driver should toggle this bit each frame, starting with a value of 1.

Bits 29-26 Reserved

Bit 30 FZ - Float Z Enable  
 0 = Fixed Z stored in z buffer in Z32 format (both 32- and 16-bit Z)  
 1 = Float Z stored in z buffer in Z32 format (both 32- and 16-bit Z)

Bit 31      ZID - Z Invert Disable (Rev. A)  
0 = 1/adjusted Z stored in z buffer  
1 = Z is not inverted by the hardware

This bit is set to 1 when the application requires that the Z Pixel Offset (BCI1D) be added to the non-inverted adjusted Z to form the value stored in the Z-Buffer (e.g., OpenGL). It is also set to one if perspective correction is turned off (BCI27\_27 = 1) and Z values are programmed into the buffer by the driver.

Bit 31      Z/W- Z/W Buffer Select (Rev. B)  
0 = Use W Buffer  
1 = Use Z Buffer

Bit 5 of this register must be set to 1 for this bit to be effective.

---

**Z-Buffer Offset Register (MM485D8) (Global)**

Read/Write                      Address: 104 85D8H  
Power-on Default: 00000000H

BCI: 33H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	R	Z-BUFFER OFFSET														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
ZBD	Z-BUFFER WIDTH						R	R	R	R	R	R	R	R	R	R

Bits 13-0      Z-BUFFER OFFSET

Value = 2K-aligned offset in frame buffer of 0,0 element of Z-Buffer

This value is padded with 11 LSB 0's to form a 24-bit address.

Bits 24-14      Reserved

Bits 30-25      Z-BUFFER WIDTH

Value = Z-Buffer width in tiles

For 16-bit tiles, this is  $((\text{width} + 3FH) \& FFC0H) \gg 6$   
For 32-bit tiles, this is  $((\text{width} + 1FH) \& FFE0H) \gg 5$

where width is the display width in pixels. 16-bit tiles are 64 pixels wide. 32-bit tiles are 32 pixels wide. Thus, for example, if the width is 640 pixels, the value = 10 (decimal) for 16-bit pixels and 20 (decimal) for 32-bit pixels.

Bit 31      ZBD - Z-Buffer Depth  
0 = 16 bits/Z coordinate  
1 = 24 bits/Z coordinate

When this bit is set to 1, each coordinate is stored in the lower 24 bits of a DWord. The upper 8 bits can be used for the stencil buffer.

**Destination Control Register (MM485DC) (Global)**

Read/Write Address: 004 85DCH  
 Power-on Default: 00000000H

BCI:34H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION OFFSET								R	DWT						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPF	AAM	R	R	R	R	R	R	R	R	DESTINATION OFFSET					

Bits 6-0 DWT - Destination Width in Tiles

Value = Destination width in tiles

For 16-bit tiles, this is  $((width + 3FH) \& FFC0H) \gg 6$   
 For 32-bit tiles, this is  $((width + 1FH) \& FFE0H) \gg 5$

where width is the destination width in pixels. 16-bit tiles are 64 pixels wide. 32-bit tiles are 32 pixels wide. Thus, for example, if the width is 640 pixels, the value = 10 (decimal) for 16-bit pixels and 20 (decimal) for 32-bit pixels.

Bit 7 Reserved

Bits 21-8 DESTINATION OFFSET

Value = Bits 24-11 of a 25-bit 2K page-aligned offset of the current destination buffer

This value is padded by the hardware with 11 LSB 0's.

Bits 28-22 Reserved

Bits 30-29 Antialiasing Mode

- 00 = Disable
- 01 = 2X
- 10 = 4X
- 11 = Reserved

Bit 31 DPF - Destination Pixel Format

- 0 = RGB565 (16-bit)
- 1 = XRGB888 (32-bit)

**Draw Control 0 Register (MM485E0) (Global)**

Read/Write Address: 004 85E0H  
 Power-on Default: 00000000H

BCI: 35H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOP SCISSORS Y				DP	LEFTMOST SCISSORS X COORDINATE										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALPHA REFERENCE								TOPMOST SCISSORS Y COORDINATE							

Bits 10-0 LEFTMOST SCISSORS X COORDINATE (inclusive)

Value = 0-based pixel count such that this is the first pixel of each line to be drawn (not clipped)

Bit 11 DP - D Performance Accelerator Enable

- 0 = Disabled
- 1 = Enabled

Bits 23-12 TOPMOST SCISSORS Y COORDINATE (inclusive)

Value = 0-based scan line count such that this is the first scan line to be drawn (not clipped)

Note: The top is line 0.

Bits 31-24 ALPHA REFERENCE



Value = 8-bit number used in alpha test comparison (Aref). Only the 5 MSBs are used.

---

**Draw Control 1 Register (MM485E4) (Global)**

Read/Write Address: 004 85E4H  
 Power-on Default: 05000000H

BCI: 36H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOTTOMMOST Y				XY	RIGHTMOST SCISSORS X COORDINATE										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EAT	ATC			BCM	NN	DE	BOTTOMMOST SCISSORS Y COORDINATE								

- Bits 10-0 RIGHTMOST SCISSORS X COORDINATE (inclusive)  
 Value = 0—based pixel count such that all pixels after this count will be clipped
- Bit 11 XY - XY Offset Enable  
 0 = Disable  
 1 = Enable
- Bits 23-12 BOTTOMMOST SCISSORS Y COORDINATE (inclusive)  
 Value = 0-base scanline count such that all lines after this count will be clipped  
 Note: The top is line 0.
- Bit 24 DE - Dither Enable  
 0 = Disable  
 1 = Enable (default)
- Bit 25 NN - Non-Normalized Texture Coordinates  
 0 = Normalized texture coordinate  
 1 = Non-normalized texture coordinate
- Bits 27-26 BCM - Backface Cull Mode  
 00 = Reserved  
 01 = Disable culling (default)  
 10 = Cull clockwise triangles  
 11 = Cull counterclockwise triangles
- Bits 30-28 ATC - Alpha Test Compare  
 000 = Never pass  
 001 = Anew < Aref  
 010 = Anew = Aref  
 011 = Anew ≤ Aref  
 100 = Anew > Aref  
 101 = Anew ≠ Aref  
 110 = Anew ≥ Aref  
 111 = Always pass
- The Aref value is programmed in MM485E0\_31-24..
- Bit 31 EAT - Enable Alpha Test  
 0 = Disable alpha test  
 1 = Enable alpha test

**Z Read/Write Watermarks Register (MM485E8) (Global)**

Read/Write Address: 004 85E8H

BCI: 37H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	Z READ HIGH WATERMARK						R	R	Z READ LOW WATERMARK					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	Z WRITE HIGH WATERMARK						R	R	Z WRITE LOW WATERMARK					

Bits 5-0 Z READ LOW WATERMARK

Value = # of Z read FIFO entries such that when the FIFO full entries value is less than this number, the Z read memory accesses priority is raised to high

Bits 7-6 Received

Bit 13-8 Z READ HIGH WATERMARK

Value = # of Z read FIFO entries such that if the FIFO full entries value is greater than this number, no Z read FIFO memory requests are issued

Bits 15-14 Reserved

Bits 21-16 Z WRITE LOW WATERMARK

Value = # of Z write FIFO entries such that when the FIFO full entries value is less than this number, no Z write FIFO memory requests are issued

If the flush pending Z writes bit (MM48584\_31) is set, this value must be all 0's. (Rev. A)

For Rev. B, these bits are effective only when the Z flush bit (MM48584\_31) is cleared to 0. If MM48584\_31 is set to 1, the Z write low watermark value must be 0.

Bits 23-22 Reserved

Bits 29-24 Z WRITE HIGH WATERMARK

Value = # of Z write FIFO entries such that if the FIFO full entries value is greater than this number, the Z write memory accesses priority is raised to high

Bits 31-30 Reserved

**3D Destination/Texture Read/Write Watermarks Register (MM485EC)**

Read/Write Address: 004 85ECH

BCI: 38H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3D DEST WRITE LWM				3D DEST READ HIGH WATERMARK						R	R	R	R	R	R
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DF		R	R	3D TEXTURE READ WM				3D DEST WRITE HIGH WATERMARK				DWLWM			

Bits 5-0 Reserved

Bit 11-6 3D DESTINATION READ HIGH WATERMARK

Value = # such that if the # of FIFO entries is greater than this watermark value, then the read will have low priority. If the # of entries is less than or equal to this value, the read will have high priority.

3D Engine Registers

Bits 17-12 3D DESTINATION WRITE LOW WATERMARK

Value = # of destination write FIFO entries such that when the FIFO full entries value is less than this number, no destination write FIFO memory requests are issued

If the flush pending destination writes bit (MM48584\_30) is set, this value must be all 0's. (Rev. A)  
 For Rev. B, these bits are effective only when the destination flush bit (MM48584\_30) is cleared to 0. If MM48584\_30 is set to 1, the destination write low watermark value must be 0.

Bits 23-18 3D DESTINATION WRITE HIGH WATERMARK

Value = # of destination write FIFO entries such that if the FIFO full entries value is greater than this number, the destination write memory accesses priority is raised to high

Bits 27-24 3D TEXTURE READ WATERMARK

Value = # of texture read FIFO entries such that when more than this number of entries are empty, the texture read priority is raised

Bits 29-28 Reserved

Bits 31-30 DF – Destination Flush

This must be programmed to 01b when destination flush is enabled (MM48584\_30 = 1).

**Texture Blending Color Register (MM485F0) (Global)**

Read/Write

Address: 00485F0H

BCI: 39H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN								BLUE							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALPHA								RED							

Bits 7-0 BLUE

Value = Blue color value

Bits 15-8 GREEN

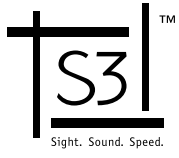
Value = Green color value

Bits 23-16 RED

Value = Red color value

Bits 31-24 Alpha

Value - Alpha color value



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## Section 11: Motion Compensation Register Descriptions

Motion compensation registers are normally accessed via the BCI. However, they can be directly accessed via memory-mapped I/O. The register identifier MM4xxxx means that the register is memory mapped at offset 004 xxxx from the base address.

---

### Motion Compensation Frame Address 0 Register (MM48900)

Read/Write Address: 004 8900H  
 Power-on Default: 00000000H

BCI: 40H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	Y DATA ADDRESS FOR PREVIOUS FRAME													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	Cb DATA ADDRESS FOR PREVIOUS FRAME													

Bits 13-0 Y DATA ADDRESS FOR PREVIOUS FRAME

Value = 2K-aligned address of the Y data frame buffer offset for the previous frame

Bits 15-14 Reserved

Bits 29-16 Cb DATA ADDRESS FOR PREVIOUS FRAME

Value = 2K-aligned address of the Cb data frame buffer offset for the previous frame

Bits 31-20 Reserved

---

### Motion Compensation Frame Address 1 Register (MM48904)

Read/Write Address: 004 8904H  
 Power-on Default: 00000000H

BCI: 41H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	Cr DATA ADDRESS FOR PREVIOUS FRAME													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	Y DATA ADDRESS FOR FUTURE FRAME													

Bits 13-0 Cr DATA ADDRESS FOR PREVIOUS FRAME

Value = 2K-aligned address of the Cr data frame buffer offset for the previous frame

Bits 15-14 Reserved

Bits 29-16 Y DATA ADDRESS FOR FUTURE FRAME

Value = 2K-aligned address of the Y data frame buffer offset for the future frame

Bits 31-20 Reserved

Motion Compensation Registers

**Motion Compensation Frame Address 2 Register (MM48908)**

Read/Write Address: 004 8908H

BCI: 42H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	Cb DATA ADDRESS FOR FUTURE FRAME													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	Cr DATA ADDRESS FOR FUTURE FRAME													

Bits 13-0 Cb DATA ADDRESS FOR FUTURE FRAME

Value = 2K-aligned address of the Cb data frame buffer offset for the future frame

Bits 15-14 Reserved

Bits 29-16 Cr DATA ADDRESS FOR FUTURE FRAME

Value = 2K-aligned address of the Cr data frame buffer offset for the future frame

Bits 31-20 Reserved

**Motion Compensation Frame Address 3 Register (MM4890C)**

Read/Write Address: 004 890CH

BCI: 43H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	Y DATA ADDRESS FOR CURRENT FRAME													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	Cb DATA ADDRESS FOR CURRENT FRAME													

Bits 13-0 Y DATA ADDRESS FOR CURRENT FRAME

Value = 2K-aligned address of the Y data frame buffer offset for the current frame

Bits 15-14 Reserved

Bits 29-16 Cb DATA ADDRESS FOR CURRENT FRAME

Value = 2K-aligned address of the Cb data frame buffer offset for the current frame

Bits 31-20 Reserved

**Motion Compensation Frame Address 4 Register (MM48910)**

Read/Write Address: 004 8910H

BCI: 44H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FW	R	Cr DATA ADDRESS FOR CURRENT FRAME													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PF	PS	PCT	FRAME HEIGHT						FRAME WIDTH (FW)						

Bits 13-0 Cr DATA ADDRESS FOR CURRENT FRAME

Value = 2K-aligned address of the Cr data frame buffer offset for the current frame

Bit 14 Reserved

Motion Compensation Registers

- Bits 20-15    FRAME WIDTH  
Value = Frame width in 16-pixel wide macroblocks
- Bits 26-21    FRAME HEIGHT  
Value = Frame height in 16-pixel high macroblocks
- Bits 28-27    PCT - Picture Coding Type  
00 = Reserved  
01 = I-picture  
10 = P-picture  
11 = B-picture
- Bits 30-29    PS - Picture Structure  
00 = Reserved  
01 = Top field  
10 = Bottom field  
11 = Frame
- Bit 31        PF - P-Type Field Picture Flag  
0 = First P-field picture  
1 = Second P-field picture

**Motion Compensation 9-bit IDCT Data Enable Register (MM48914)**

Read/Write                      Address: 004 8914H    BCI: 45H  
Power-on Default: 00000000H

This register applies only to the inter-macroblock. 9-bit IDCT must be enabled via MM48928\_27. If a block is not coded, the enable bit has no effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	Y0	Y1	Y2	Y3	Cb	Cr
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Bit 0        Cr 9-bit Enable  
0 = 8-bit IDCT data  
1 = Expand IDCT data to 9 bits
- Bit 1        Cb 9-bit Enable  
0 = 8-bit IDCT data  
1 = Expand IDCT data to 9 bits
- Bit 2        Y3 9-bit Enable  
0 = 8-bit IDCT data  
1 = Expand IDCT data to 9 bits
- Bit 3        Y2 9-bit Enable  
0 = 8-bit IDCT data  
1 = Expand IDCT data to 9 bits
- Bit 4        Y1 9-bit Enable  
0 = 8-bit IDCT data  
1 = Expand IDCT data to 9 bits
- Bit 5        Y0 9-bit Enable  
0 = 8-bit IDCT data  
1 = Expand IDCT data to 9 bits  
1 = Y0 block coded
- Bits 31-6    Reserved

Motion Compensation Registers

**Motion Vector 0 Register (MM48918)**

Read/Write Address: 004 8918H

BCI: 46H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	MOTION VECTOR 0 HORIZONTAL COMPONENT											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	FS	R	R	MOTION VECTOR 0 VERTICAL COMPONENT									

Bits 11-0 MOTION VECTOR 0 HORIZONTAL COMPONENT

Value = Horizontal component of: (half pixel unit)

First forward motion vector [0][0] or  
Dual-prime motion vector @ same parity [0][0]

Bits 15-12 Reserved

Bits 25-16 MOTION VECTOR 0 VERTICAL COMPONENT

Value = Vertical component of: (half pixel unit)

First forward motion vector [0][0] or  
Dual-prime motion vector @ same parity [0][0]

Bits 27:26 Reserved

Bit 28 FS - Motion Vector [0][0] Field Select  
0 = Top reference field  
1 = Bottom reference field

This bit applies only to non-dual-prime field prediction.

Bits 31-29 Reserved

**Motion Vector 1 Register (MM4891C)**

Read/Write Address: 004 891CH

BCI: 47H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	MOTION VECTOR 1 HORIZONTAL COMPONENT											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	FS	R	R	MOTION VECTOR 1 VERTICAL COMPONENT									

Bits 11-0 MOTION VECTOR 1 HORIZONTAL COMPONENT

Value = Horizontal component of: (half pixel unit)

Second forward motion vector [1][0] or  
First dual-prime motion vector @ opposite parity [2][0]

Bits 15-12 Reserved

Bits 25-16 MOTION VECTOR 1 VERTICAL COMPONENT

Value = Horizontal component of: (half pixel unit)

Second forward motion vector [1][0] or  
First dual-prime motion vector @ opposite parity [2][0]

Bits 27-26 Reserved



---

Motion Compensation Registers

Bit 28 FS - Motion Vector [1][0] Field Select  
 0 = Top reference field  
 1 = Bottom reference field

This bit applies only to non-dual-prime field prediction.

Bits 31-29 Reserved

---

**Motion Vector 2 Register (MM48920)**

Read/Write Address: 004 8920H  
 Power-on Default: 00000000H

BCI: 48H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	MOTION VECTOR 2 HORIZONTAL COMPONENT											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	FS	R	R	MOTION VECTOR 2 VERTICAL COMPONENT									

Bits 11-0 MOTION VECTOR 2 HORIZONTAL COMPONENT

Value = Horizontal component of: (half pixel unit)

First backward motion vector [0][1] or  
 Second dual-prime motion vector @ opposite parity [3][0]

Bits 15-12 Reserved

Bits 25-16 MOTION VECTOR 2 VERTICAL COMPONENT

Value = Vertical component of: (half pixel unit)

First backward motion vector [0][1] or  
 Second dual-prime motion vector @ opposite parity [3][0]

Bits 27-26 Reserved

Bit 28 FS - Motion Vector [0][1] Field Select  
 0 = Top reference field  
 1 = Bottom reference field

This bit applies only to non-dual-prime field prediction.

Bits 31-29 Reserved

---

**Motion Vector 3 Register (MM48924)**

Read/Write Address: 004 8924H  
 Power-on Default: 00000000H

BCI: 49H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	MOTION VECTOR 3 HORIZONTAL COMPONENT											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	FS	R	R	MOTION VECTOR 3 VERTICAL COMPONENT									

Bits 11-0 MOTION VECTOR 3 HORIZONTAL COMPONENT

Value = Horizontal component of second backward motion vector [1][1](half pixel unit)

Bits 15-12 Reserved

---

**Motion Compensation Registers**


---

Bits 25-16 MOTION VECTOR 3 VERTICAL COMPONENT

Value = Vertical component of second backward motion vector [1][1](half pixel unit)

Bits 27-26 Reserved

Bit 28 FS - Motion Vector [1][1] Field Select

0 = Top reference field

1 = Bottom reference field

This bit applies only to non-dual-prime field prediction.

Bits 31-29 Reserved

---

**Macroblock Description Register (MM48928)**

Read/Write Address: 004 8928H

BCI: 4AH

Power-on Default: 00000000H

Writing this register via MMIO when BCI is disabled automatically kicks off decoding of a macroblock. This is used for testing.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACROBLOCK ROW (MR)					MOTION		MBT		DCT	Y0	Y1	Y2	Y3	Cb	Cr
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	9B	MV0	MV1	MV2	MV3	MACROBLOCK COLUMN					MR	

Bit 0 Cr  
0 = Not coded  
1 = Cr block coded

Bit 1 Cb  
0 = Not coded  
1 = Cb block coded

Bit 2 Y3  
0 = Not coded  
1 = Y3 block coded

Bit 3 Y2  
0 = Not coded  
1 = Y2 block coded

Bit 4 Y1  
0 = Not coded  
1 = Y1 block coded

Bit 5 Y0  
0 = Not coded  
1 = Y0 block coded

NOTE: Bits 5-0 apply only to the inter-macroblock.

Bit 6 DCT -DCT Type  
0 = Frame DCT  
1 = Field DCT

Bits 8-7 MBT - Macroblock Type  
00 = Intra  
01 = Forward, inter  
10 = Backward, inter  
11 = Backward, forward, inter

Motion Compensation Registers

---

Bits 10-9      MOTION - Motion Type  
                   00 = Reserved  
                   01 = Field  
                   10 = Frame (or 16x8 MC)  
                   11 = Dual prime

Bits 16-11    MACROBLOCK ROW

Value = Y coordinate in units of macroblocks

This is  $(mb\_addr/mb\_width)$ , using integer division with truncation towards 0.

Bits 22-17    MACROBLOCK COLUMN

Value = X coordinate in units of macroblocks

This is  $(mb\_addr \bmod mb\_width)$

Bit 23        MV3 - Motion Vector 3 Enable  
                   0 = Motion vector 3 disabled  
                   1 = Motion vector 3 enabled

Bit 24        MV2 - Motion Vector 2 Enable  
                   0 = Motion vector 2 disabled  
                   1 = Motion vector 2 enabled

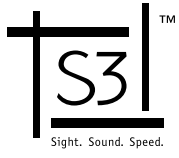
Bit 25        MV1 - Motion Vector 1 Enable  
                   0 = Motion vector 1 disabled  
                   1 = Motion vector 1 enabled

Bit 26        MV0 - Motion Vector 0 Enable  
                   0 = Motion vector 0 disabled  
                   1 = Motion vector 0 enabled

Bit 27        9B - 9-bit IDCT Enable  
                   0 = 9-bit IDCT disabled  
                   1 = 9-bit IDCT enabled

Bits 31-28    Reserved

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## Section 12: Mastered Data Transfer Register Descriptions

Mastered Data Transfer registers are normally accessed via the BCI. However, they can be directly accessed via memory-mapped I/O. The register identifier MM4xxxx means that the register is memory mapped at offset 004 xxxx from the base address.

---

### Mastered Data Transfer Control Register (MM48A00) - MIT/Pixel Formatter/Motion Compensation Modes

Read/Write Address: 004 8A00H  
 Power-on Default: 00000000H

BCI: 50H

A write to this register with BCI disabled initiates the selected transfer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRANSFER LENGTH/STRIDE												CMD TYPE			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TD	420 DISP	CS	ST	FM	SRC PF	DEST PF	TRANSFER LENGTH								

Bits 2-0 CMD TYPE - Command Type  
 000 = Motion compensation data  
 010 = Mastered image transfer  
 011 = Pixel formatter

All other values reserved.

Bits 20-3 TRANSER LENGTH/STRIDE

MIT Value = [# of QWord units to be transferred] -1  
 Motion Compensation Value - [# of QWord units to be transferred] -1] - bits 5-3 must be 111 (8QWord-aligned)  
 Formatter Value (linear) = Address offset between vertically adjacent (frame or 420 field) scan lines  
 Formatter Value (tiled) - Address offset between vertically adjacent page stripes

Bits 22-21 DEST PF - Destination Pixel Format (Formatter only)  
 00 = Reserved  
 01 = YCbCr422 packed  
 10 = RGB565  
 10 = XRGB8888

Bits 24-23 SRC PF - Source Pixel Format (Formatter only)  
 00 = YCbCr420 planar  
 01 = YCbCr422 packed  
 10 = RGB565  
 10 = XRGB8888

Bits 26-25 FM - Formatter Mode for Oversampling  
 00 = No oversampling  
 01 = 2X  
 10 = 4X  
 11 = Reserved

This function can only be used with tiled RGB565 frame buffer data as the source. The destination must be tiled RGB565 or XRGB8888 in the frame buffer. This function cannot be enabled simultaneously with color space conversion.

Bit 27 ST - Source Tiling (valid only if frame buffer is source)  
 0 = Source is not tiled  
 1 = Source is tiled

Mastered Data Transfer Registers

- Bit 28 CS - Color Space Conversion Enable (Formatter only)  
 0 = Disable  
 1 = Enable
- This function cannot be enabled simultaneously with oversampling (bits 26-25).
- Bits 30-29 420 DISP - 420 Display (Formatter only)  
 00 = Frame to frame  
 01 = Frame to field  
 10 = Field to frame  
 11 = Field to Field
- This applies only to YCbCr420 source. It affect both luma and chroma data.
- Bit 31 TD - Transfer Direction  
 0 = System memory to frame buffer  
 1 = Frame buffer to system memory
- This bit applies only to mastered image transfers.

**Mastered Data Transfer Control Register (MM48A00) - Command DMA Mode**

Read/Write Address: 004 8A00H BCI: 50H  
 Power-on Default: 00000000H

A write to this register with BCI disabled initiates a command DMA transfer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRANSFER COUNT											CMD TYPE				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	TRANSFER COUNT				

- Bits 2-0 CMD TYPE - Command Type  
 100 = Command DMA
- All other values reserved.
- Bits 20-3 TRANSFER COUNT
- Value = [Transfer size in QWords] - 1
- Bits 31-21 Reserved

**Mastered Data Transfer Control Register (MM48A00) - Vertex Mode**

Read/Write Address: 004 8A00H BCI: 50H  
 Power-on Default: 00000000H

A write to this register with BCI disabled initiates a vertex data transfer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START ADDRESS										BT	MT	CMD TYPE			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START ADDRESS															

- Bits 2-0 CMD TYPE - Command Type  
 001 = Vertex fetching
- All other values are reserved.

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**Mastered Data Transfer Registers**


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Bit 3 MT - Memory Type  
 0 = Frame buffer  
 1 = System memory

Bit 4 BT - Bus Type  
 0 = PCI  
 1 = AGP

This bit must be cleared to 0 when bit 3 of this register is cleared to 0.

Bits 31-5 START ADDRESS

Value = 4 QWord-aligned start address for vertex data to be transferred.

If the data are in the frame buffer, only bits 24-5 are used.

---

**Mastered Data Transfer Source/Luma Address Register (MM48A04)**

Read/Write Address: 004 8A04H  
 Power-on Default: 00000000H

BCI: 51H

This register applies to mastered image, pixel formatter, motion compensation and command DMA transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOURCE ADDRESS											QWR	R	SMT	SL	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SOURCE ADDRESS															

Bit 0 SL - Source Location  
 0 = Source is in frame buffer memory  
 1 = Source is in system memory

Bit 1 SMT - System Memory Type  
 0 = Source is in PCI memory (physically contiguous and page-locked)  
 1 = Source is in AGP memory

This bit must be cleared to 0 if the source is in frame buffer memory.

Bit 2 Reserved

Bits 4-3 QWR - 420 QWord Resolution

Value = QWord resolution used in bits 31-5 of this register for YCbCr420 source data mode only. Otherwise, these bits are reserved.

Bits 31-5 SOURCE ADDRESS

Value = 4 QWord-aligned starting address of the entire source bitmap

For frame buffer memory, only bits 24-5 are valid.

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Mastered Data Transfer Registers

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**Mastered Data Transfer Destination Address Register (MM48A08)**

Read/Write Address: 004 8A08H

BCI: 52H

Power-on Default: 00000000H

This register applies to mastered image and formatter transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIT DESTINATION ADDRESS											R	R	R	SMT	SL
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIT DESTINATION ADDRESS															

Bit 0 DL - Destination Memory Location  
0 = Destination is in frame buffer memory  
1 = Destination is in system memory

Writes to system memory are not supported for AGP systems.

Bits 4-1 Reserved

Bits 31-5 MIT DESTINATION ADDRESS

Value = 4 QWord-aligned starting address of the entire destination bitmap

For frame buffer memory, only bits 24-5 are valid.

---

**Mastered Data Transfer Formatter Source Dimensions Register (MM48A0C)**

Read/Write Address: 004 8A0CH

BCI: 53H

Power-on Default: 00000000H

This register applies to pixel formatter transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	SOURCE WIDTH									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	SOURCE HEIGHT										

Bits 9-0 SOURCE WIDTH  
Value = Source width - 1 in QWords

2 pixel aligned for XRGB8888 (4 pixel aligned if destination is 16bpp)

4 pixel aligned for RGB565

16 pixel aligned for YCbCr

Bits 15-10 Reserved

Bits 26-16 SOURCE HEIGHT

Value = Source height -1 in lines

Bits 31-27 Reserved



Mastered Data Transfer Registers

**Mastered Data Transfer Formatter Destination Dimensions Register (MM48A10)**

Read/Write Address: 004 8A10H

BCI: 54H

Power-on Default: 00000000H

This register applies to pixel formatter transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	STRIDE WIDTH													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	DT

Bits 13-0 STRIDE WIDTH

Value = Destination stride in QWords

Bits 15-14 Reserved

Bit 16 DT - Destination Tiling  
 0 = linear (not tiled)  
 1 = tiled

This bit applies only when the destination is an RGB format in the frame buffer.

Bits 31-17 Reserved

**Mastered Data Transfer Source/Cb Address Register (MM48A14)**

Read/Write Address: 004 8A14H

BCI: 55H

Power-on Default: 00000000H

This register applies to YCbCr420 formatter transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOURCE/Cb ADDRESS											QWR	R	SMT	SL	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SOURCE/Cb ADDRESS															

Bit 0 SL - Source Location  
 0 = Source is in frame buffer memory  
 1 = Source is in system memory

Bit 1 SMT - System Memory Type  
 0 = Source is in PCI memory (physically contiguous and page-locked)  
 1 = Source is in AGP memory

This bit must be cleared to 0 if the source is in frame buffer memory.

Bit 2 Reserved

Bits 4-3 QWR - 420 QWord Resolution

Value = QWord resolution used in bits 31-5 of this register.

Bits 31-5 SOURCE/Cr ADDRESS

Value = 4 QWord-aligned starting address of the Cb data for YCbCr420 conversion

For frame buffer memory, only bits 24-5 are valid.

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Mastered Data Transfer Registers

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**Mastered Data Transfer Source/Cr Address Register (MM48A18)**

Read/Write Address: 004 8A18H

BCI: 56H

Power-on Default: 00000000H

This register applies to YCbCr420 formatter transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOURCE/Cr ADDRESS											QWR	R	SMT	SL	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SOURCE/Cr ADDRESS															

Bit 0 SL - Source Location  
0 = Source is in frame buffer memory  
1 = Source is in system memory

Bit 1 SMT - System Memory Type  
0 = Source is in PCI memory (physically contiguous and page-locked)  
1 = Source is in AGP memory

This bit must be cleared to 0 if the source is in frame buffer memory.

Bit 2 Reserved

Bits 4-3 QWR - 420 QWord Resolution

Value = QWord resolution used in bits 31-5 of this register.

Bits 31-5 SOURCE/Cr ADDRESS

Value = 4 QWord-aligned starting address of the Cr data for YCbCr420 conversion

For frame buffer memory, only bits 24-5 are valid.

---

**Mastered Data Transfer Source Cr/Cb Strides Register (MM48A1C)**

Read/Write Address: 004 8A1CH

BCI: 57H

Power-on Default: 00000000H

This register applies to pixel formatter YCbCr420 transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cr MAP SOURCE STRIDE													R	R	R
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Cb MAP SOURCE STRIDE													R	R	R

Bits 2-0 Reserved

Bits 15-3 Cr MAP SOURCE STRIDE

Value = Source stride in QWords of the Cr map

For linear data, this is the address offset between vertically adjacent pixels. For tiled data, this is the address offset between vertically adjacent page strips. The maximum stride is 64KB.

Bits 18-16 Reserved

Bits 31-19 Cb MAP SOURCE STRIDE

Value = Source stride in QWords of the Cb map

For linear data, this is the address offset between vertically adjacent pixels. For tiled data, this is the address offset between vertically adjacent page strips. The maximum stride is 64KB.

## Section 13: Configuration/Status Register Descriptions

Configuration/status registers are accessed directly via memory-mapped I/O. The register identifier MM4xxxx means that the register is memory mapped at offset 004 xxxx from the base address. Two registers (Vertex Buffer Address and BCI Power Management) also have a BCI address.

### Status Word 0 Register (MM48C00) (Rev A)

Read Only                      Address: 004 8C00H  
 Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FILLED COMMAND BUFFER ENTRIES (FE)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	PF	MEI	R	MCI	2DI	3DI	BI	FE

- Bits 16-0      FILLED COMMAND BUFFER ENTRIES  
 Value = # of filled positions in the command queue  
 The number includes filled positions in both the on-chip and overflow buffers.
- Bit 17        BI - BCI Idle  
 0 = Not idle  
 1 = Idle
- Bit 18        3DI - 3D Graphics Engine Idle  
 0 = Not idle  
 1 = Idle
- Bit 19        2DI - 2D Engine Idle  
 0 = Not idle  
 1 = Idle
- Bit 20        MCI - Motion Compensation Processor Idle  
 0 = Not idle  
 1 = Idle
- Bit 21        Reserved
- Bit 22        MEI - Master Engine Idle  
 0 = Not idle  
 1 = Idle
- Bit 23        PF - Page Flip Pending  
 0 = Not pending  
 1 = Pending
- Bits 31-24    Reserved

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Configuration/Status Registers

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**Status Word 0 Register (MM48C00) (Rev B)**

Read Only                      Address: 004 8C00H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FILLED COMMAND BUFFER ENTRIES (FE)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PF	MEI	R	MCI	2DI	3DI	BI	R	R	R	R					FE

Bits 20-0      FILLED COMMAND BUFFER ENTRIES

Value = # of filled (DWORD) positions in the command queue

The number includes filled positions in both the on-chip and overflow buffers. The LSB of this field now reads 1 from the time the counter hits the upper threshold until just before its hits the lower threshold on the way down. When the counter hits the lower threshold, the LSB changes to 0 and remains in that state until just before it reaches the upper threshold on the way up.

Bits 24-21      Reserved

Bit 25          BI - BCI Idle  
0 = Not idle  
1 = Idle

Bit 26          3DI - 3D Graphics Engine Idle  
0 = Not idle  
1 = Idle

Bit 27          2DI - 2D Engine Idle  
0 = Not idle  
1 = Idle

Bit 28          MCI - Motion Compensation Processor Idle  
0 = Not idle  
1 = Idle

Bit 29          Reserved

Bit 30          MEI - Master Engine Idle  
0 = Not idle  
1 = Idle

Bit 31          PF - Page Flip Pending  
0 = Not pending  
1 = Pending

---

**Status Word 1 Register (MM48C04)**

Read Only                      Address: 004 8C04H

Power-on Default: 00000000H

The event tag values in this register is passed as part of an UpdateShadowStatus BCI command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVENT TAG 0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EVENT TAG 1															

Bits 15-0      EVENT TAG 0

Value = 16-bit event tag reporting the status of command parsing at the time of an update shadow status request is reached by the parser

Configuration/Status Registers

Bits 31-16 EVENT TAG 1

Value = 16-bit event tag reporting the status of command parsing at the time of an update shadow status request is reached by the parser

**Status Word 2 Register (MM48C08)**

Read Only Address: 004 8C08H  
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL RETRACE COUNT					SCAN LINE NUMBER										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	VERT RETRACE

Bits 10-0 SCAN LINE NUMBER

Value = Number of the scan line currently being refreshed

Bits 18-11 VERTICAL RETRACE COUNT

Value = 8-bit vertical retrace counter current value

An 8-bit counter is incremented each vertical retrace. The counter rolls over to 0 when it reaches its maximum.

Bits 31-19 Reserved

**Shadow Status Address Register (MM48C0C)**

Read/Write Address: 004 8C0CH  
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADOW STATUS ADDRESS											R	R	R	R	SUE
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHADOW STATUS ADDRESS															

Bit 0 SUE - Status Update Enable  
0 = Disable updating the shadow status in system memory  
1 = Enable updating the shadow status in system memory

BCI must be disabled when this bit is set. Updates are generated either by an UpdateShadowStatus BCI command or by passing a threshold programmed in MM48C10 (assuming MM48C18\_1 = 1).

Bits 4-1 Reserved

Bits 31-5 SHADOW STATUS ADDRESS

Value = Bits 31-5 of the physical address of Status Word 0 in locked system memory

This value is padded with five 0's by the hardware (32-byte aligned).

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Configuration/Status Registers

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**Command Buffer Thresholds Register (MM48C10)**

Read/Write Address: 004 8C10H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND BUFFER STOP WRITE (UPPER) THRESHOLD															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMMAND BUFFER RESUME WRITE (LOWER) THRESHOLD															

Bits 15-0 COMMAND BUFFER STOP WRITE (UPPER) THRESHOLD

Value = # of command queue entries empty in DWORDs (Rev. A) or 32 DWORD units (Rev. B)

When this many 32-bit queue entries are used (both on- and off-chip ) and MM8C18\_2 = 1 and MM8C0C\_0 = 1, the Shadow Status in system memory is updated to indicate that the CPU must stop register writes. Software reads bits 16-0 of Status Word 0 to determine the number of entries. This update occurs only as the threshold is passed as the queue is filling. This value must be greater than the resume write threshold in bits 31-16 of this register.

Bits 31-16 COMMAND BUFFER RESUME WRITE (LOWER) THRESHOLD

Value = # of command queue entries in DWORDs (Rev. A) or 32 DWORD units (Rev. B)

When this many 32-bit queue entries are used (both on- and off-chip) and MM8C18\_2 = 1 and MM8C0C\_0 = 1, the Shadow Status in system memory is updated to indicate that the CPU can resume register writes. Software reads bits 16-0 of Status Word 0 to determine the number of entries. This update occurs only as the threshold is passed as the queue is emptying. This value must be less than the stop write threshold in bits 16-0 of this register.

**Command Overflow Buffer Register (MM48C14)**

Read/Write (See bits) Address: 004 8C14H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	COMMAND OVERFLOW BUFFER OFFSET													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COB SIZE			WC	R	R	R	R	R	R	R	R	R	R	R	R

Bits 13-0 COMMAND OVERFLOW BUFFER OFFSET (Read/Write)

Value - Bits 24-11 of the address offset of the command overflow buffer in the frame buffer

This value is padded with eleven 0's by the hardware (2K-aligned).

Bits 27-14 Reserved

Bit 28 WC – Write Combining Enable

0 = Write combining disabled

1 = Write combining enabled

When write combining is enabled, the driver must ensure that there is no address gap within 32 BCI entries (addresses must be consecutive)

Configuration/Status Registers

Bits 31-29 COB SIZE - COMMAND OVERFLOW BUFFER SIZE (Read/Write) (Rev. A)  
 000 = 256 entries (2KB address alignment)  
 001 = 512 entries (2KB address alignment)  
 010 = 1K entries (4KB address alignment)  
 011 = 2K entries (8KB address alignment)  
 100 = 4K entries (16KB address alignment)  
 101 = 8K entries (32KB address alignment)  
 110 = 16K entries (64KB address alignment)  
 111 = 32K entries (128KB address alignment)

Each entry uses 4 bytes. This buffer is enabled via MM48C18\_2.

Bits 31-29 COB SIZE - COMMAND OVERFLOW BUFFER SIZE (Read/Write) (Rev. B)  
 000 = 8K entries  
 001 = 16K entries  
 010 = 32K entries  
 011 = 64K entries  
 100 = 128K entries  
 101 = 256K entries  
 110 = 512K entries  
 111 = 1M entries

**Command Overflow Buffer Pointers Register (MM48C18)**

Read/Write Address: 004 8C18H  
 Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CBE	R	CMD OVERFLOW POINTER					R	R	R	R	R	BE	OQE	CSU	R	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
COMMAND BUFFER ENTRIES (CBE)																

Bit 0 Reserved

Bit 1 CSU - Command Buffer Status Update  
 0 = Command buffer status update disabled  
 1 = Command Buffer status update enabled

Updating is based on the thresholds in MM48C10. MM8C0C\_0 must also be set to 1 for this update to occur.

Bit 2 OQE - Command Overflow Buffer Enable  
 0 = Overflow command circular buffer disabled  
 1 = Overflow command circular buffer enabled

Bit 3 BE - BCI Enable  
 0 = BCI function disabled  
 1 = BCI function enabled

This bit affects all BCI functions.

Bits 8-4 Reserved

Bits 13-9 CMD OVERFLOW POINTER

Value = # of commands and MMIO register writes in the command overflow buffer

Bit 14 Reserved

Bits 31- 15 COMMAND BUFFER ENTRIES

Value = # of entries (on and off chip) in the command buffer

Configuration/Status Registers

**Vertex Buffer Address Register (MM48C20)**

Read/Write Address: 104 8C20H

BCI: 3EH

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTEX BUFFER ADDRESS											R	R	R	SMT	SL
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTEX BUFFER ADDRESS															

Bit 0 SL - Vertex Buffer Location  
 0 = Vertex buffer is in frame buffer memory  
 1 = Vertex buffer is in system memory

Bit 1 SMT - System Memory Type  
 0 = Vertex buffer is in PCI memory (physically contiguous and page-locked)  
 1 = Vertex buffer is in AGP memory

This bit must be cleared to 0 if the source is in frame buffer memory.

Bits 4-2 Reserved

Bits 31-5 VERTEX BUFFER ADDRESS

Value = 4 QWord-aligned address of the start of the vertex buffer

For frame buffer memory, only bits 23-5 are valid.

**BCI Power Management Register (MM48C24)**

Read/Write Address: 004 8C24H

BCI: 5FH

Power-on Default: 00000000H

With automatic clock management and BCI operation enabled for a particular block, the clock to that block is turned off when the block is idle. With automatic clock management for a block disabled, the clock is turned on/off by the corresponding control bit (one of bits 8-11 of this register).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	MT	MC	2D	3D	R	R	R	R	AMT	AMC	A2D	A3D
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 A3D - Automatic 3D Engine Clock Management Enable  
 0 = Automatic 3D engine clock management disabled (use bit 8 to enable/disable clock)  
 1 = Automatic 3D engine clock management enabled (disable clock when engine idle)

Bit 1 A2D - Automatic 2D Engine Clock Management Enable  
 0 = Automatic 2D engine clock management disabled (use bit 9 to enable/disable clock)  
 1 = Automatic 2D engine clock management enabled (disable clock when engine idle)

Bit 2 AMC - Automatic Motion Compensation Engine Clock Management Enable  
 0 = Automatic motion compensation engine clock management disabled (use bit 10 to enable/disable clock)  
 1 = Automatic motion compensation engine clock management enabled (disable clock when engine idle)

Bit 3 AMT - Automatic Mastered Transfer Engine Clock Management Enable  
 0 = Automatic mastered transfer engine clock management disabled (use bit 11 to enable/disable clock)  
 1 = Automatic mastered transfer engine clock management enabled (disable clock when engine idle)

Bits 7-4 Reserved

Bit 8 3D - 3D Engine Clock Enable  
 0 = Clock to 3D Engine enabled  
 1 = Clock to 3D Engine disabled



Configuration/Status Registers

- Bit 9      2D - 2D Engine Enable  
0 = 2D Engine disabled  
1 = 2D Engine enabled
- Bit 10     MC - Motion Compensation Engine Enable  
0 = Motion Compensation Engine disabled  
1 = Motion Compensation Engine enabled
- Bit 11     MT - Mastered Transfer Engine Enable  
0 = Mastered Transfer Engine disabled  
1 = Mastered Transfer Engine enabled
- Bits 31-12   Reserved

**Tiled Surface Register (MM48C40, MM48C44, MM48C48, MM48C4C, MM48C50)**

Read/Write                      Address: 004 8C40H  
Power-on Default: 00000000H

For address mapping 0 (CRB0\_7 = 1), all five of the tiled surface registers listed above are defined by this register and apply to Tile Surface Address Aperture 0-4 respectively. For address mapping 1 (CRB0\_7 = 0), only MM48C40, MM48C44 and MM48C48 are valid and apply to Tiled Surface Address Aperture 0-2 respectively.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
TILED SURFACE FRAME BUFFER OFFSET																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
BPP		YF	S3TC			TILED SURFACE WIDTH										

Bits 19-0      TILED SURFACE FRAME BUFFER OFFSET  
  
Value = 4-QWord-aligned address offset in the frame buffer  
  
This alignment can be used for texture surfaces. 2K-alignment (2 additional LSB 0's) must be used for the Z-Buffer and draw buffers.

Bits 25-20     TILED SURFACE WIDTH  
  
Value = Surface width in tiles  
  
For 4 bits, this (width + 3FH) >>6  
  
For 8 and 16-bit tiles, this is ((width + 3FH) & FFC0H) >> 6  
  
For 32-bit tiles, this is ((width + 1FH) & FFE0H) >> 5  
  
where width is the surface width in pixels. 4-, 8- and 16-bit tiles are 64 pixels wide. 32-bit tiles are 32 pixels wide. Thus, for example, if the width is 640 pixels, the value = 10 (decimal) for 8- and 16-bit pixels and 20 (decimal) for 32-bit pixels.

Bits 28-26     S3TC - S3TC Surface Width  
000 = 64 pixels or less  
001 = 128 pixels  
010 = 256 pixels  
011 = 512 pixels  
100 = 1024 pixels  
101 = 2048 pixels  
110 = Reserved  
111 = Reserved

Bit 29         YF - Y Range Flag  
0 = Y range is from 23:13 for 8-bit and 32-bit format, from 23:12 for 16-bit format and from 23:14 for 4-bit format  
1 = Y range is from 23:12 for 32-bit format and from 23:11 for 16-bit format

Configuration/Status Registers

Bits 31-30 BPP - Tiled Surface Bits/Pixel  
 00 = 4 bits/pixel  
 01 = 8 bits/pixel  
 10 = 16 bits/pixel  
 11 = 32 bits/pixel

**Alternate Status Word 0 Register (MM48C60) (Rev. A)**

Read Only Address: 004 8C60H  
 Power-on Default: 00000000H

This register provides the same information as MM48C00.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FILLED COMMAND BUFFER ENTRIES (FE)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	PF	MEI	R	MCI	2DI	3DI	BI	FE

Bits 16-0 FILLED COMMAND BUFFER ENTRIES  
 Value = # of filled positions in the command queue  
 The number includes filled positions in both the on-chip and overflow buffers.

Bit 17 BI - BCI Idle  
 0 = Not idle  
 1 = Idle

Bit 18 3DI - 3D Graphics Engine Idle  
 0 = Not idle  
 1 = Idle

Bit 19 2DI - 2D Engine Idle  
 0 = Not idle  
 1 = Idle

Bit 20 MCI - Motion Compensation Processor Idle  
 0 = Not idle  
 1 = Idle

Bit 21 Reserved

Bit 22 MEI - Master Engine Idle  
 0 = Not idle  
 1 = Idle

Bit 23 PF - Page Flip Pending  
 0 = Not pending  
 1 = Pending

Bits 31-24 Reserved

**Alternate Status Word 0 Register (MM48C60) (Rev B)**

Read Only                      Address: 004 8C60H

Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FILLED COMMAND BUFFER ENTRIES (FE)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	PF	MEI	R	MCI	2DI	3DI	BI	FE

Bits 16-0      FILLED COMMAND BUFFER ENTRIES

Value = # of filled positions in the command queue

The number includes filled positions in both the on-chip and overflow buffers.

Bit 17      BI - BCI Idle  
0 = Not idle  
1 = Idle

Bit 18      3DI - 3D Graphics Engine Idle  
0 = Not idle  
1 = Idle

Bit 19      2DI - 2D Engine Idle  
0 = Not idle  
1 = Idle

Bit 20      MCI - Motion Compensation Processor Idle  
0 = Not idle  
1 = Idle

Bit 21      Reserved

Bit 22      MEI - Master Engine Idle  
0 = Not idle  
1 = Idle

Bit 23      PF - Page Flip Pending  
0 = Not pending  
1 = Pending

Bits 31-24    Reserved

**Alternate Status Word 1 Register (MM48C64)**

Read Only                      Address: 004 8C64H

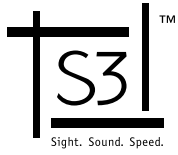
Power-on Default: 00000000H

This register provides the same information as MM48C04

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTEX BUFFER TAG															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CURRENT TEXTURE SURFACE TAG															

Bits 15-0      EVENT TAG

Value = 16-bit event tag reporting the status of command parsing at the time of an update shadow status request is reached by the parser



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Configuration/Status Registers

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Bits 31-16 CURRENT TEXTURE SURFACE TAG

Value = 16-bit texture surface counter current value

A 16-bit counter is incremented each time the Texture Address register (MM485C4) is updated. The DirectDraw driver uses this to synchronize re-use of surface memory through LockSurface.

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# Index

<b>1</b>		
1.5V		
auto adjust of drive.....	54, 55	
pad compensation.....	54	
1280x1024x24 support .....	87	
<b>2</b>		
24 bpp packed .....	151	
2D Engine		
enable .....	89	
2D Graphics Engine		
axial step constant .....	136	
background color.....	140	
background/foreground mix .....	142	
bitplane read mask.....	141	
bitplane write mask .....	140	
clipping.....	146	
clock select .....	134	
color compare .....	141, 146	
color source.....	142, 143	
command types.....	139	
current X position .....	136	
current Y position .....	135	
destination base address .....	145	
destination X position .....	137	
destination Y position.....	136	
diagonal step constant .....	137	
drawing direction .....	138	
enable .....	134	
enable 8 bpp or greater.....	76	
foreground color .....	140	
idle status.....	223, 224, 230, 231	
line error term.....	137	
major axis pixel count.....	147	
memory mapping .....	71	
minor axis pixel count.....	143	
scissors .....	144	
screen width .....	82	
select mix register .....	145	
short stroke vector.....	139	
software reset.....	133	
source base address.....	145	
<b>3</b>		
32 bits/pixel operation .....	146	
3D engine		
scissors .....	204	
3D Engine		
backface cull mode .....	205	
color compare .....	190, 191, 199	
command buffer entries .....	223, 224, 230, 231	
destination control .....	204	
Enable .....	89, 134	
fog control .....	200	
fog table registers.....	199	
idle status.....	223, 224, 230, 231	
mipmapping.....	190, 191	
texture address .....	192, 193	
texture control .....	190, 191	
texture description.....	197	
texture surface tag .....	232	
texture transparency .....	190, 191	
texture transparent color .....	197	
vertex buffer tag .....	224, 225, 231	
Z buffering control .....	201, 202	
<b>4</b>		
4 bank SDRAM support .....	103	
<b>A</b>		
AD bus		
drive control.....	98	
AGP		
2x clock skew control .....	111	
4x capability .....	108	
clock select .....	75	
clock skew.....	47, 48, 88	
clocking .....	126	
command priority select .....	93	
command register .....	126	
command suspend.....	93	
enable .....	75, 126	
FIFO status .....	126	
IDSEL.....	75	
PLL bypass .....	74	
PLL powerdown .....	48	
side band addressing enable .....	126	
sideband addressing support.....	94	
status register.....	125	
stop SB_STB.....	93	
suspend mode.....	93	
voltage select .....	108	
alpha blending.....	156	

Configuration/Status Registers

**B**

- backface cull mode ..... 205
- BCI ..... 4
  - command circular buffer..... 227
  - enable ..... 227
  - enable (2D) ..... 148
  - global bitmap descriptor ..... 148
  - interrupt ..... 131, 132, 133
  - power management ..... 228
  - primary bitmap descriptor..... 149
  - secondary bitmap descriptor ..... 150
- bilinear decimation ..... 180, 181
- BIOS ROM
  - data ..... 105
  - flash ROM address ..... 104
  - programmability..... 74
  - serial versus parallel ..... 108, 187, 188
- bits/pixel
  - color depth ..... 82
- BLANK pedestal enable ..... 48
- blank/border select..... 72
- blending ..... 155
- block write
  - enable 1 cycle operation ..... 100
- burst command interface..... 4
- bus master enable..... 114
- byte mode addressing ..... 23
- byte swap ..... 139

**C**

- capabilities list pointer ..... 123
- character clock
  - dot clocks per ..... 9
- chip ID ..... 70, 71
- chroma keying ..... 151, 153
- clipping
  - 2D..... 146
  - 2D disable ..... 146
- clock generator
  - new DCLK PLL load ..... 43
  - new ECLK PLL load ..... 50
  - new MCLK and DCLK PLL load ..... 44
  - new MCLK PLL load ..... 43
- CLUT
  - 18- or 24-bit select ..... 47
- color compare ..... 146
  - 2D graphics ..... 141, 146
  - 3D..... 190, 191, 199
  - 3D enable..... 190, 191
  - VGA..... 26, 29
- color depth (bpp) ..... 82
- color keying ..... 151
  - in KRGB mode ..... 152
  - on color index..... 152

- command buffer
  - registers ..... 226
  - thresholds..... 226
- command circular buffer
  - overflow buffer enable..... 227
- configuration strapping
  - unlocking access to registers ..... 76
- CPU base address
  - enable ..... 71
  - specify ..... 91
- cursor
  - end ..... 17
  - location address ..... 18
  - start ..... 17
  - update policy ..... 79

**D**

- D2 PCI management state enable ..... 78
- DAC
  - internal reference current adjust ..... 49
- DCLK
  - control ..... 47
  - external input..... 75
  - external output ..... 44
  - halving..... 9, 44
  - invert ..... 44
  - inverted ..... 72
  - loading new frequency ..... 43, 44
  - PLL M parameter ..... 42, 53
  - PLL N parameter ..... 41, 52
  - PLL R parameter ..... 41, 52
  - programming ..... 41, 42, 52, 53
- DDC communications ..... 109
- decimation ..... 179
- destination base address ..... 145
- display active status..... 6
- display FIFO fetch
  - enable ..... 73
  - specify start position ..... 77
- display memory
  - refresh cycle control ..... 20
  - size specification ..... 74
  - type select ..... 91
- display pitch ..... 20
- display start address ..... 91
- double buffering
  - select..... 159
- doubleword mode addressing ..... 20, 21, 71
- drive control ..... 98

<b>E</b>	<b>H</b>
ECLK	hardware graphics cursor
IREF control ..... 50	background color..... 81
loading new frequency ..... 50	enable ..... 79
enable	fix for flat panel display ..... 55
hardware graphics cursor..... 79	foreground color ..... 80
linear addressing..... 84, 134	pattern display x origin ..... 81
LPB ..... 171	pattern display y origin ..... 82
PCI bus master operation ..... 114	storage start address ..... 81
video display ..... 7, 135	Windows/X-Windows modes..... 84
end horizontal blank..... 13	x origin..... 80
end horizontal sync position..... 14	y origin..... 80
end vertical blank ..... 22	HDTV support ..... 152
	high speed text display ..... 71
<b>F</b>	high speed text font writing ..... 76
FIFO fetch delay..... 100	horizontal blank
flat panel	end ..... 13
centering and expansion for 15/16 or 32 bpp.... 102	start ..... 13
detect ..... 50	horizontal decimation type ..... 172
display enable positioning..... 60	horizontal display enable
hardware cursor fix..... 55	delay..... 88
horizontal centering..... 56	horizontal display end ..... 13
horizontal expansion ..... 56	horizontal downscaling mode..... 153
horizontal expansion factor ..... 59	horizontal expansion
panel detect..... 50	alternate ..... 56
PanelLink 12/24-bit interface..... 50	horizontal sync
strapping bit..... 108	control for power management ..... 40
sync positioning ..... 61	polarity..... 5
vertical centering ..... 57	horizontal sync position
vertical expansion ..... 57	end ..... 14
vertical expansion factor ..... 60	start ..... 14
flicker filter	horizontal total..... 12
odd/even field status ..... 72	HSYNC
fog	skew by character clocks ..... 15
control ..... 200	
fog table registers ..... 199	<b>I</b>
	I/O access
<b>G</b>	disable..... 74
gamma correction	enable ..... 114
enable ..... 47	I2C port ..... 104
set CLUT for 24-bit operation..... 47	add wait states ..... 175
genlock support..... 152	ID, chip ..... 70, 71
global bitmap descriptor	interlaced operation ..... 77, 79
registers ..... 148	interrupt
select..... 82	2D Graphics Engine busy interrupt status..... 131
GOPO ..... 86	2D Graphics Engine interrupt enable ..... 132
GPOUT	enable ..... 72
pin state control..... 40	FIFO empty interrupt enable ..... 132
green PC	FIFO empty interrupt status ..... 131
HSYNC/VSYNC control..... 40	FIFO overflow interrupt enable..... 132
	FIFO overflow interrupt status..... 131
	LPB ..... 174
	vertical retrace interrupt clear..... 19

Configuration/Status Registers

vertical retrace interrupt enable..... 19, 131, 132  
 vertical retrace interrupt status..... 6  
 interrupt pin claimed..... 124

**L**

L parameter..... 102, 103  
 latency timer..... 116  
 LCLK  
   invert ..... 172  
 line compare..... 23  
 linear addressing  
   bypass VGA logic..... 39  
   enable ..... 84, 134  
   window position. 117, 118, 119, 120, 121, 122, 123  
   window size..... 84  
 live video  
   tearing ..... 101  
 Local Peripheral Bus  
   LBP ..... 171  
 LPB  
   bilinear decimation ..... 180, 181  
   color byte swap ..... 171  
   decimation..... 179  
   enable ..... 171  
   frame buffer address..... 175, 180  
   horizontal decimation type ..... 171  
   input window size..... 178  
   interrupt ..... 132  
   interrupts ..... 174  
   line stride..... 179  
   live video data mirroring..... 172  
   mode select..... 171  
   odd/even field detect..... 172  
   omit stride..... 171  
   output FIFO..... 173, 180  
   quadlinear decimation ..... 181  
   reset ..... 171  
   skip frames..... 171  
   sync polarity ..... 171  
   VBI enable..... 182  
   VBI parameters ..... 182, 183, 184  
   video FIFO ..... 172, 173  
   VSYNC indicator ..... 175  
   write priority..... 101  
 LUT write cycle control..... 45

**M**

MA bus  
   drive strength ..... 98  
 macroblock description ..... 211, 214  
 master abort..... 115  
 mastered image transfer  
   registers ..... 219  
 mastered image transfers

control ..... 217, 218  
 engine idle status ..... 223, 224, 230, 231  
 maximum scan line ..... 16  
 MCLK  
   external output ..... 43  
   loading new frequency ..... 43, 44  
   programming ..... 40, 41, 51  
   use external input..... 74  
 memory mapped access  
   enable ..... 114  
 memory mapped I/O  
   MMIO only select ..... 39  
 memory mapping  
   Enhanced/VGA modes..... 71  
 mipmapping..... 190, 191  
 MMIO  
   chip wakeup ..... 135  
   memory mapped I/O..... 83  
 motion compensation  
   engine idle status ..... 223, 224, 230, 231  
   macroblock description ..... 211, 214  
   registers ..... 209

**N**

nibble swap ..... 83

**O**

offset ..... 20  
 overflow command circular buffer  
   enable ..... 227

**P**

pad compensation..... 54  
 palette registers ..... 32  
   lock access ..... 72  
 panning ..... 16, 33, 34  
 pattern fill ..... 139  
 PCI bus  
   bus master enable..... 114  
   bus master latency timer ..... 116  
   maximum latency ..... 124  
   minimum grant ..... 124  
   received master abort ..... 115  
   received target abort ..... 115  
   subvendor ID..... 123  
 PCI Bus  
   BIOS ROM access enable ..... 123  
   BIOS ROM base address..... 123  
   capabilities list..... 114  
   capabilities list pointer..... 123  
   capability identifier ..... 125  
   disable read bursts..... 76  
   enable disconnect..... 89





Configuration/Status Registers

streams processor		gain adjust.....	48
blending.....	155	output level.....	46
chroma keying.....	153	two page screen.....	71
color/chroma keying.....	151		
compose modes.....	156	<b>U</b>	
display FIFO fetch delay .....	100	underline location.....	21
display FIFO fetch timing .....	100	unlocking	
double buffering .....	157, 158	configuration strapping registers.....	76
FIFO control .....	163	extended sequencer registers.....	39
filter characteristics .....	151, 152	S3 VGA registers .....	75
filter constants.....	154	system control/extension registers.....	76
input data formats .....	151, 153		
mode select.....	90	<b>V</b>	
primary stream stride .....	157	VBI	
primary stream window .....	163	enable .....	182
register loading.....	89	parameters .....	182, 183, 184
scaling.....	161, 162	VCLK	
secondary stream stride.....	161, 168	phase with respect to DCLK.....	90
secondary stream window.....	164	vertex buffer address .....	228
switch display buffer between VSYNCs .....	156	vertical blank	
subsystem ID .....	123	end .....	22
information source select .....	75	start .....	21
shadow CR registers.....	96, 99	vertical display end .....	20
		vertical expansion[alternate] .....	58
<b>T</b>		vertical interpolation	
target abort.....	115	enable .....	162
texture		luma only.....	153
address .....	192, 193	vertical retrace	
control .....	190, 191	counter value.....	225
current surface tag .....	232	enable interrupt .....	19
description.....	197	end .....	19
transparency .....	190, 191	start .....	19
transparent color .....	197	vertical sync	
tiled surface definition .....	229	active status .....	7
tiling		control for power management .....	40
primary stream on/off .....	157	polarity.....	5
secondary stream on/off.....	161	vertical total .....	15
timeout registers.....	94	VGA graphics mode select.....	32
triple buffering .....	156	VGA memory bus width .....	71
select.....	159	VGA memory mapping.....	71, 72
tri-state off		video BIOS	
HSYNC.....	84	access enable (PCI).....	123
VSYNC.....	84	base address (PCI) .....	123
TV		video display enable .....	31
8 bpp modes .....	52	VIP	
8 bpp output .....	52	control .....	176
DAC output level .....	46	device select .....	176
enable digital data output.....	50	power down.....	185
encoder mode .....	52	timeout .....	185
external encoder strapping.....	108	VSYNC	
return clock phase.....	50	change buffer between.....	156
TVCLK delay.....	52		
use flat panel logic .....	49		
TV DAC			
control .....	46, 51		

## W

wakeup.....	135
watermarks	
3D destination/texture read/write .....	206
primary stream .....	165
secondary stream.....	166
Z read/write .....	206
word mode addressing.....	20, 22, 23
write blocking	
enable software control.....	169
write combining enable .....	226

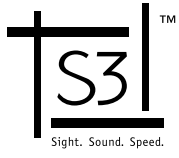
## X

X-Windows.....	84
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## Z

Z buffering	
control .....	201, 202
offset .....	203

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