HEWLETT hp PACKARD

MEMORY PARITY CHECK for 2114A COMPUTER

model 12598A

OPERATING AND SERVICE MANUAL 1 FEB 1969

1. MEMORY PARITY CHECK.

2. Memory Parity Check option Model 12598A provides the HP 2114A Computer with "odd" parity (an odd total of true bits, including the parity bit, in each computer memory word). The parity of all words transferred from memory is also checked. If a bit is either dropped or added in the transfer process, a parity error indication is generated. The manner in which the Computer responds to the parity error is selectable by the user (by reversing the top connector on the Parity Error board). The Computer may be set to the halt mode, which halts the Computer and lights the front panel PARITY indication, or it may be set to the interrupt mode in which the Computer interrupts to location 5 in addition to giving the PARITY indication. The address of the memory location containing the parity error is stored and may be loaded into the A, B, or S Registers for identification regardless of the mode of operation. The use of a parity error subroutine accessed through interrupt location 5 allows the computer user to correct the lost or added bit and then return to the main program at the point at which the parity error occurred.

3. INSTALLATION.

4. Installation of the option is easily accomplished in the field with one plug-in unit, Parity Error printed circuit board 12598-6001. This board may be installed in the factory when ordered as part of the initial computer system. To install Memory Parity Check option HP 12598A, perform the following:

a. Make certain that the computer POWER switch is in the "off" position.

b. Install the Parity Error printed circuit board in slot A5 of the HP 2114A. The components mounted on the board should face to the left as you face the front of the Computer.

c. Install the top connector, 12580-6002 on the top edge of the board. When this connector is in the normal position (extractor handle aligned with those of adjacent connectors), the Parity Halt function is enabled. When the top connector is installed in the reverse position (extractor handle off-set with respect to adjacent connectors) the Computer will interrupt on detection of a parity error.

d. If there is no subroutine to service the interrupt, location 5 should contain a HLT instruction.

e. If the Computer has previously been run without the parity error board it will be necessary to correct the parity bits in memory. The Basic Binary Loader should have its parity bits corrected first to facilitate the correction of other programs stored in memory. This may be done by putting the LOADER PROTECT switch in the ENABLED position. Load the starting address of the Basic Binary Loader program (the last 64 locations in memory) and step through the Loader program using the DISPLAY MEMORY button. Return the LOADER PROTECT switch to NORMAL position and reload any programs that were stored in memory. The Parity Error circuits will automatically assign the correct parity to any programs loaded. If the Computer is run for even a short time with the Parity Error board removed, all programs that have been stored in memory should be reloaded to assign proper parity.

5. OPERATION.

6. Operation of the Memory Parity Check option is completely automatic during normal Computer operation and requires no special attention by the Computer operator. The option may be operated in the Parity Error Halt mode or in the Parity Error Interrupt mode. The Parity Error Interrupt mode is enabled by reversing the 48-pin top connector of the Parity Error board. If a parity error occurs during the Computer's operation it is recommended that the complete program be reloaded before resuming normal Computer operation. However, it is possible to continue Computer operation without reloading the program (see Paragraph 10).

7. HALT FUNCTION. When the 48-pin top connector is in the normal position the Halt mode of the option is enabled. If a parity error occurs the parity error card will cause the Computer to halt, as indicated by the illumination of the PARITY lamp on the Computer front panel. In this case the option does not cause an interrupt of the Computer program but halts at the location following the error instead. Again, it is recommended that the complete program be reloaded. However, if it should be desired to continue the program in operation without reloading, proceed in the following manner:

a. First ensure that the instruction executed during the parity error has not altered the contents of any of the registers or the contents of any memory location. To do this, read the information contained in the T-Register as visible on the Computer front panel and check the phase status of this information. By using this data and a program listing it is possible

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to determine what operations have taken place during execution of the information that had the parity error. Affected memory locations may now be checked, and any errors may be corrected by loading the proper data into the respective memory locations.

b. After correcting the parity error and any register or memory contents that it may have affected return the Computer to the location in the program at which the parity error occurred and resume normal operation.

8. INTERRUPT FUNCTION. When the top connector described above is reversed, the Parity Error Interrupt mode is enabled. The Parity Error card will then cause an interrupt to location 00005 (octal) on detecting a parity error. Memory location 00005 may contain any type of instruction as desired by the Computer user. The interrupt capability of the Parity Error Interrupt card is enabled when Computer power is turned on, and unlike external I/O devices does not have to be initialized by the computer program. However, if desired by the Computer user, the interrupt capability of the Parity Error card may be reinitialized by program control following the occurrence of a parity error interrupt by use of an STF 05 instruction in a parity error subroutine. Table 1 provides a sample interrupt subroutine (a JSB instruction referencing the subroutine is assumed to be stored in location 00005) which could be used to automatically present both the offending data and its program location to the Computer user. Again the same procedure used in the Halt mode (Paragraph 7) should be used to ensure that the parity error has not affected other parts of the program or data. When this check is complete, normal operation may be resumed.

9. PARITY ERROR ADDRESS. The memory address at which the parity error occurred is stored in the Parity Error Address Register on the Parity Error card. By using LIA 5 and OTA 1 (Load Into the A-Register the contents of the Parity Error Address Register and Output the contents of the A-Register to the S-Register) the address of the parity error can be read on the front panel.

10. It may be desirable to continue operation without reloading the complete program. To do this, use the following procedure:

a. Using the address of the parity error obtained in Paragraph 9 above, determine what operations have taken place during the execution of the instruction that experienced the parity error. Affected memory locations may be checked, and any errors may be corrected by loading the proper information into the proper memory locations. It may also be necessary to correct the program if it too has been affected by the error.

b. Now with the Computer in the same state that it was in when the error occurred it is possible to resume normal operation.

11. THEORY OF OPERATION.

12. BASIC OPERATION.

13. In order to ensure that the total number of true bits in each Computer word is always odd, it is necessary to control the value (true or false) of the parity bit. The Parity Error card does this by monitoring the T-Register bits to determine if each Computer word (16 bits plus the parity bit) transferred from memory, has an odd number of true bits. If even parity is detected, an error signal is generated on the Parity Error card which interrupts or halts Computer operation as determined by the placement of the 48-pin connector on the Parity Error card.

Table 1. Sample Parity Error Interrupt Subroutine

LABEL	OPCODE	OPERAND	COMMENTS
PESR	NOP		Enter P.E. Subroutine
	STA	SVA	Save the contents of the A-Register
	STB	SVB	Save the contents of the B-Register
	LIA	01	Load the contents of the S-Register
	STA	SVS	Save the contents of the S-Register
	LIA	5	Load the address of the P.E.
	AND	RSET	Reset the Parity indicator bit (15)
	LDB	0,1	Load the incorrect data into B-Register
	OTA	01	Display the address of the P.E.
	HLT		
	OTB	01	Display the incorrect data
	HLT		Correct the data, Register and Memory contents affected by P.E.
	LIB	01	Load corrected data into B-Register
	STB	00,I	Store corrected data
	LDA	SVS	
	OTA	01	Restore S-Register
	LDA	SVA	Restore A-Register
	LDB	SVB	Restore B-Register
	STF	5	Turn on P.E. Interrupt
	JMP	PESR,I	Exit P.E. Subroutine
RSET	OCT	077777	

14. PARITY CALCULATING NETWORK. The purpose of the Parity Calculating Network is to determine whether the sum of all true bits in the T-Register is odd or even, during both the read and write operations. It produces one output signal, $\overline{TR16}$. During write operations if the number of bits in the T-Register, not including the parity bit (TR16), is odd then $\overline{TR16}$ will be high indicating that the number of true bits held in the T-Register is odd without need of a true parity bit. Similarly if the number of bits in the T-Register is even the $\overline{TR16}$ signal will go false writing a true parity bit into memory at T5 to provide odd parity in the memory word. During read operations, the $\overline{TR16}$ signal generated by the Parity Calculating Network is compared with the previously stored parity bit for that memory word. The Parity Bit Flip-Flop is set by an $\overline{ST16}$ signal, which is generated on the Sense Amplifier board during the memory read cycle, and causes the Parity Bit Flip-Flop to follow the state of the parity bit read out of memory. MC12D/E and F compare the parity bit read out of memory and the parity bit generated by the Parity Calculating Network. If the two disagree, a false $\overline{\text{Parity Error}}$ signal is generated indicating an error.

15. In order to simplify explanation of the Parity Calculating Network, Figure 1 has been provided to show its basic operation by using only two input data signals. The resulting output signifies whether the sum of true bits in a hypothetical 2-bit T-Register is odd or even. This output, now the new parity bit, is checked with the previously stored parity bit to generate a Parity Error signal (Paragraph 14).

16. Refer to Figure 1 while reading the following circuit explanation. In Figure 1, "and" gate MC43D in the Parity Calculating Network receives the TR0 and TR1 signals from the T-Register as input data signals. If both of these signals are true, there will be a true output to "nor" gate MC43F indicating that there is an even number of true bits in the T-Register (11). Inverting gates MC32C and MC32D provide $\overline{TR0}$ and $\overline{TR1}$ inputs to "and" gate MC43E. If both of these inputs are true there will be a true output to "nor" gate MC43F indicating an even number of true bits in the T-Register (00). If either of the inputs to "nor" gate MC43F is true the gate will output a false $\overline{TR16}$ signal to memory to generate odd parity during the "write" operation or to the Error Detect Logic to indicate an even sum of bits during the read operation. If both "nor" gate inputs are false (01 or 10) a true $\overline{TR16}$ signal will be generated to maintain odd parity during the memory write operation and to indicate an odd sum of bits to the Error Detect Logic during the memory read operation. During the memory read cycle the $\overline{TR16}$ signal is compared with the contents of the Parity Bit Flip-Flop MC102A in the Error Detect Logic.

17. During memory read operations, the Error Detect Logic MC22C and MC12D/E/F performs a comparison between what the T-Register contents indicate the parity bit should be and the actual state of the parity bit stored in memory. To do this the output bit of the Parity Bit Sense Amplifier, $\overline{ST16}$, is applied to the Parity Bit Flip-Flop, MC102A. This signal, if false (true parity bit in memory), sets the flip-flop and is applied as a true input to pin 1 of MC12D and a false (inhibit) input to MC12E. The sum of data bits must therefore be even to inhibit MC12D. With a true $\overline{TR16}$ signal from the Parity Calculating Network (odd sum) applied to pin 13 of MC12D, a true

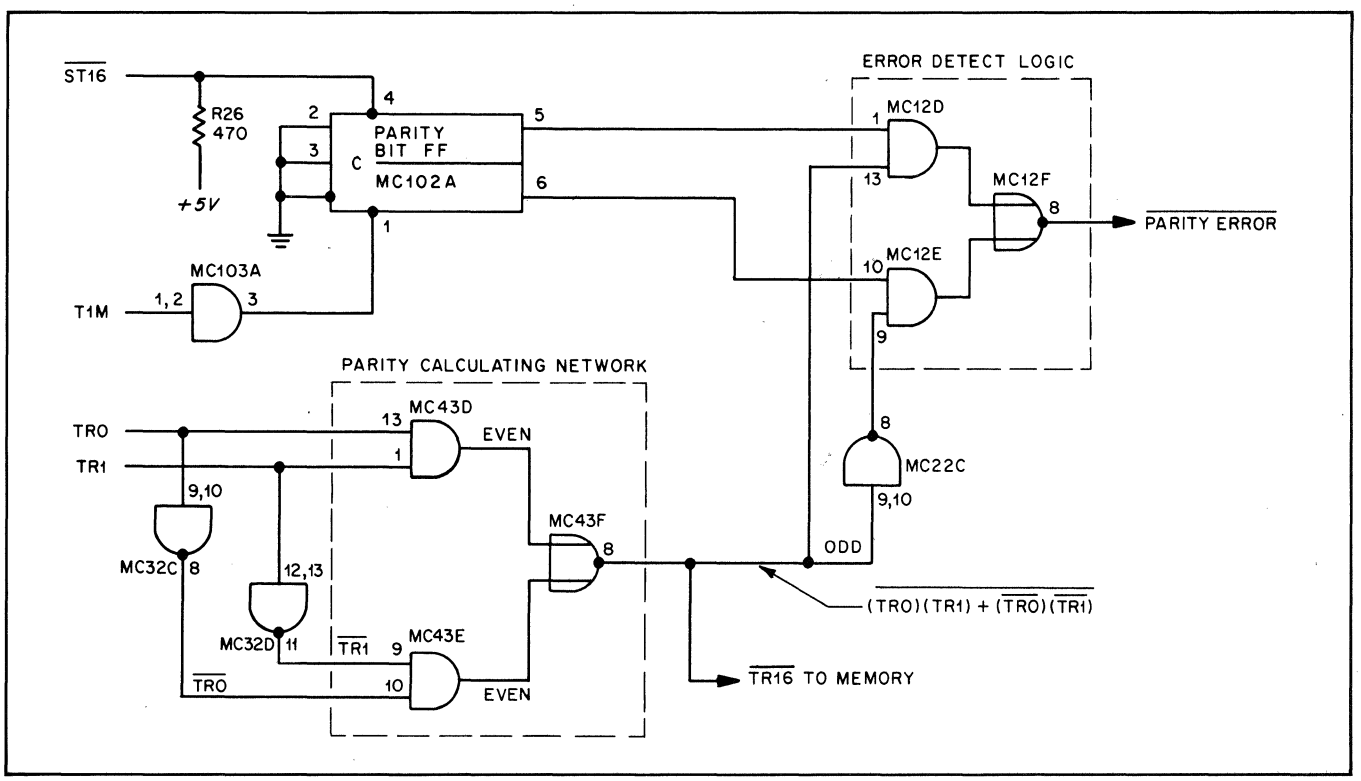

Figure 1. Simplified Parity Calculating Network

input will be applied to "nor" gate MC12F giving a false $\overline{PE}$ signal indicating a parity error. A false $\overline{TR16}$ signal from the Parity Calculating Network (even sum) applied to pin 13 of MC12D will cause a false input to be applied to "nor" gate MC12F and provides a true $\overline{PE}$ signal at pin 8 of MC12F indicating no parity error.

18. DETAILED LOGIC.

19. PARITY ERROR SIGNAL. (Refer to Figure 3, Parity Error Interrupt card.) Table 2 summarizes the functions of command lines to the Parity Error card. When a true input is applied to either input of "nor" gate MC12F a false $\overline{PE}$ signal (a parity error), is generated. A false input is then applied to "nor" gate MC76E. In order for the output of MC76E to be true, propagating the Parity Error signal, the following conditions must first exist:

a. Either the ISZ (Increment and Skip if Zero) signal and the PH3 (Phase 3) signal applied to pins 2 and 1 of MC73A respectively must be true causing a false input to pin 1 of MC76C or the MWL (Memory Write Level) signal applied to pin 13 of MC76C must be false, providing a false input to "nor" gate MC76E. This allows the parity to be checked during the ISZ instruction, which utilizes a normal memory read cycle.

b. Both the AAF (A Addressable Flip-Flop) and the BAF (B Addressable Flip-Flop) signals, pins 55 and 56, must be false. This prevents the generation of extraneous parity errors during AAF or BAF operations since the A and B registers do not contain a stored parity bit.

Table 2. Control Signals to the Parity Error Card

CONTROL SIGNALS	DESCRIPTION
IOG, SCM(0), SCL(5)	Enables control commands to the Parity Error card.
STF(05)	Enables the interrupt capability of the Parity Error card.
CLF(05)	Disables the interrupt capability of the Parity Error card.
IAK	Will reset the Parity Error Flag at time T1 following a parity interrupt to prevent more than one interrupt from the same parity error.
IOI(05)	Generated by an input group instruction with the Select Code 05; allows retrieval of the address of the parity error.

20. When the conditions described above are met, a true output signal is obtained on pin 8 of MC76E and applied to pin 3 of MC75A. When MTE is true (MTE is normally true except when the Loader Enable switch is in the NORMAL position and the LOAD Flip-Flop is clear) and timing signal T3 is true the three inputs to MC75A are all true, giving a false $\overline{PE}$ output. The false $\overline{PE}$ signal goes to pin 11 of MC102B to clock in $\overline{M12}$, the most significant bit of the parity error address. The $\overline{PE}$ is also inverted by MC103C and D and sent to pins 4 and 13 of each of quad-latching flip-flops MC96, 106, and 26. These flip-flops then clock in the remaining bits of the parity error address. Since the "not" outputs of the M-Register are used to provide the input data to the Parity Error Address Register, the address bits are taken from the reset sides of the address flip-flops when the address is retrieved.

21. The true PE signal from MC103C is also applied to pin 2 of MC84A. The false output resets the Flag Buffer Flip-Flop. If the Computer is set for the Halt mode, the output of the Flag Buffer Flip-Flop is inverted by MC42C and sent as a false $\overline{PEH}$ signal to halt the Computer. The output of the Flag Buffer Flip-Flop is also sent to enable MC84D (Flag gate) and to provide a true input to MC74B (Interrupt Request gate). The Flag Flip-Flop is set via MC84D by the ENF (T2) signal in the machine phase following the resetting of the Flag Buffer Flip-Flop. The output of the Flag Flip-Flop causes the PEI (Parity Error Indicator) signal to go true, turning on the PARITY indicator on the Computer front panel. The true output of the Flag Flip-Flop is also used to provide a true input to MC73B. The other input is provided by the set Control Flip-Flop. This gives a false output to MC85A, breaking the priority signal to the I/O Control card to keep interrupts from other devices from being generated. It also provides a false input to MC22D. MC22D then provides a true output to pin 9 of MC74B (the second of four required enabling signal for interrupt request). At time T5 the SIR signal from the Timing Generator card goes true (third signal), and a high PRL 4 signal from the I/O Control card (fourth signal) sets the IRQ Flip-Flop, generating the IRQ5 signal. This signal is inverted by MC42B to form a false $\overline{PINT}$ signal to the I/O Control card. The set IRQ Flip-Flop puts a true input on pin 2 of MC92A. At T1 of the next machine phase the IAK signal makes the other input of MC92A true resetting the Flag Buffer Flip-Flop. The false output from the Flag Buffer Flip-Flop results in a true output from MC74B. This allows the IRQ Flip-Flop to be reset by the ENF (T2) signal from the Timing Generator card.

22. INTERRUPT IDENTIFICATION. When a Parity Error occurs and causes an interrupt to memory location 00005 (octal), the instruction contained in location 00005 may tell the Computer to execute a subroutine. Contained in the subroutine must be an LIA, MIA, LIB, or MIB instruction which when executed causes a true IOI signal input to pin 64 of the Parity Error card to be applied to pin 6 of MC85B. At the same time execution of one of these instructions causes the SCM0 (Select Code Most significant digit 0), SCL5 (Select Code Least significant digit 5), and the IOG signals from pins 59, 66, and 57 respectively to go true. This causes a true output from "and" gate MC86C, since PEI (Parity Error Indicator signal) is also true. MC85B then provides a true output to enable the output gates MC83A/B, MC15A/B, MC16A/B,

MC105A/B, MC104A/B, MC95A/B, and MC94A/B of the Parity Error Address Register. This allows the address of the parity error to be read onto the IOB (Input/Output Bus) line under program control. MC83A outputs a true bit 15 onto the IOB line whenever the contents of the Parity Error Address Register are read. Bit 15 is used to indicate that the address is that of a parity error.

23. CLF. The CLF (Clear Flag signal at pin 32 of the Parity Error card becomes true when a CLF instruction is executed during the Parity Error Interrupt subroutine. This signal is applied to pin 10 of MC73D. This causes the Control Flip-Flop to be reset putting a false input on pin 4 of MC73B. The output of MC84B provides the other false input to MC73B. The true output of MC73B causes MC22D to provide a false input to MC74B. This action inhibits the interrupt circuitry during the execution of the interrupt subroutine.

24. STF. The STF (Set Flag) signal at pin 19 of the Parity Error card becomes true when an STF instruction is executed by the interrupt subroutine. This signal together with the 05 Select Code causes MC72D to output a false signal to MC75C of the Flag Flip-Flop and MC74A of the Flag Buffer Flip-Flop, enabling the interrupt system. The STF 05 instruction also provides a true input to MC72B, causing a false input to MC75A of the Control Flip-Flop. This causes a true output from the Control Flip-Flop to pin 4 of MC73B, enabling the interrupt request circuits.

25. POPIO. When the Computer power is turned on, or whenever the PRESET button on the Computer front panel is pushed, the POPIO (Power On Pulse to the I/O section) signal is applied to pin 45 of the Parity Error card. In order to initialize the card's interrupt capability, the inverted POPIO signal is applied to the following places:

a. Pin 13 of MC75A to set the Control Flip-Flop.

b. Pin 11 of MC75C to set the Flag Flip-Flop.

c. Pin 1 of MC74A to set the Flag Buffer Flip-Flop.

26. REPLACEABLE PARTS.

27. Table 3 lists replaceable parts in alphanumeric order of their reference designations, with a description and HP part number for each part. Figure 2 shows the location of all parts on the Parity Error board. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office.

Table 3. Replaceable Parts List

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR. CODE	MFR. PART NO.	QTY
C1-40	0150-0093	C:fxd cer 0.01 uf, +80-20%, 100 VDCW	91418	TA	40
C41-43	0180-0155	C:fxd elect 2.2 uf, 20%, 20 VDCW	56289	150D225X0020A2-DYS	2
C44	0160-0938	C:fxd, Mica, 1000 pf, 5%	72136	RDM15E102J1C	1
MC12,13,24,35,36, 43,45,46	1820-0378	Integrated Circuit: TTL	28480	1820-0378	8
MC14,22,23,25,32 33,34,44	1820-0370	Integrated Circuit: TTL	28480	1820-0370	8
MC15,16,83,85,93, 94,95,104,105	1820-0974	Integrated Circuit: CTL	28480	1820-0974	9
MC26,96,106	1820-0301	Integrated Circuit: TTL	28480	1820-0301	3
MC42	1820-0327	Integrated Circuit: TTL	28480	1820-0327	1
MC72,73,84,92,103	1820-0054	Integrated Circuit: TTL	28480	1820-0054	5
MC74	1820-0069	Integrated Circuit: TTL	28480	1820-0069	1
MC75	1820-0068	Integrated Circuit: TTL	28480	1820-0068	1
MC76	1820-0074	Integrated Circuit: TTL	28480	1820-0074	1
MC86	1820-0973	Integrated Circuit: TTL	28480	1820-0973	1
MC102	1820-0077	Integrated Circuit: TTL	28480	1820-0077	1
R26,31,41,42,44, 45,48	0683-4715	R:fxd comp 470 ohm, 5% 1/4W	01121	CB 4715	7
R34,43,49,50,51, 52	0683-1025	R:fxd comp 1K, 5%,1/4W	01121	CB 1025	6
R40,46,54	0683-1525	R:fxd comp 1.5K, 5%, 1/4W	01121	CB 1525	3
R47	0683-4705	R:fxd comp 47 ohm, 5%, 1/4W	01121	CB 4705	1
W3,5	8159-0005	Jumper: Wire, Insulated	04404		2

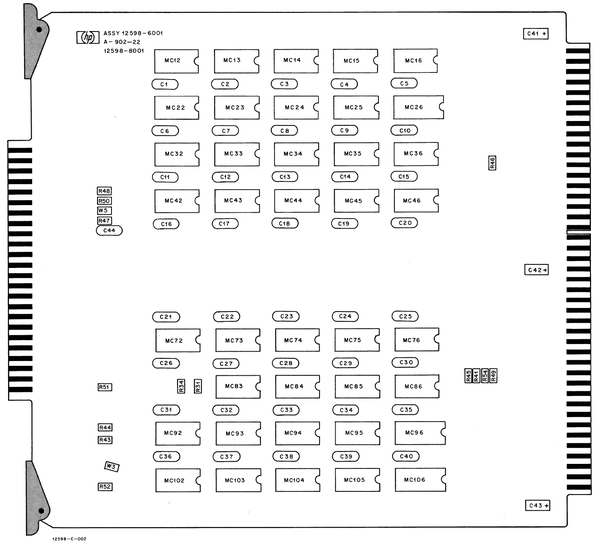

Figure 2. Part Location Diagram

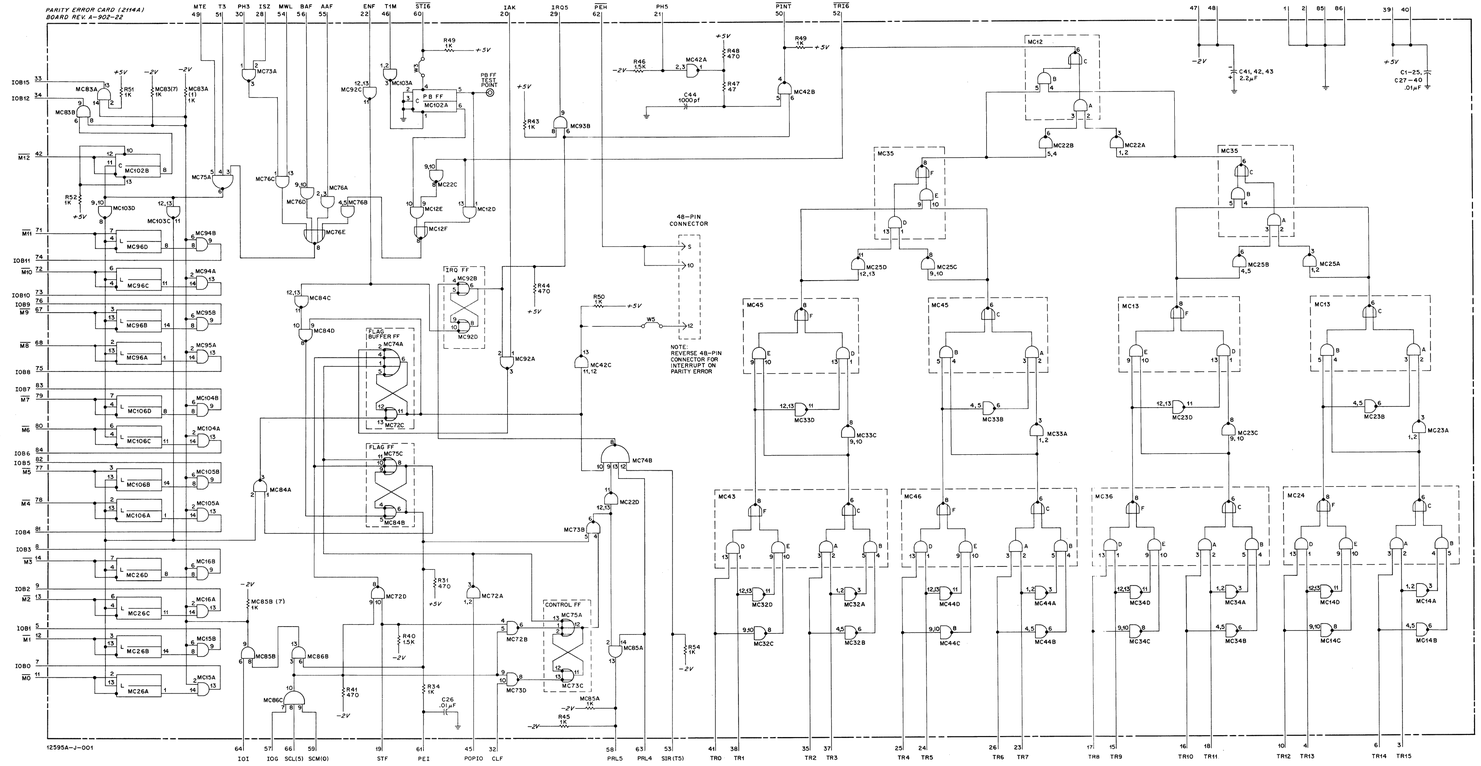

Figure 3. Parity Error Interrupt Card

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DIAGNOSTIC TEST AND PROCEDURE for MEMORY PARITY CHECK

model 12598A

DIAGNOSTIC SUPPLEMENT 5 FEB 1969

1. INTRODUCTION.

2. The information contained in this supplement provides the computer user with procedures for testing the operation of the Memory Parity Check Option HP 12598A. By performing these diagnostic tests the user can determine which circuits and functions of the option are operating correctly and which are malfunctioning. This supplement is to be used in conjunction with the 12598A Memory Parity Check operating manual.

3. MEMORY PARITY CHECK DIAGNOSTIC.

4. Memory Parity Check diagnostic, HP 20345A, furnishes the computer user with a method of testing the operational and programmable features of Memory Parity Check. The routine includes 17 separate checks of the Parity Error card operation. (Order information for the diagnostic tape is contained in Paragraph 24 of this supplement.)

5. TEST PROCEDURE.

6. Make certain that the Computer POWER switch is in the "OFF" position. The Parity Error board should be properly installed in slot A5 with the components facing to the left from the front of the Computer. Place the top connector hood in the Interrupt position. Restore power to the Computer. Load all zeros (NOP) in location 00005 to permit loading the diagnostic tape without generating unwanted parity halts. This procedure also assigns proper parity to the Basic Binary Loader program if this has not already been done.

7. When the loading of the diagnostic tape is complete, turn off power to the Computer and remove the Parity Error board in order to insert parity errors into memory for test purposes. Restore power to the Computer and press the PRESET button. Set the address to 7000 (octal) and press RUN. This sets up data patterns with both correct and incorrect parity bits for use later in the test. The Computer should halt with the T-Register set to 102072.

8. A jumper should now be placed from pin 52 (TR16) of slot A5 to ground. This will cause a true bit 16 to be written back into memory for each word read out regardless of the word's true parity. When a machine with a 4K memory is used set Switch Register bit 15. Press the PRESET and RUN buttons. The Computer should halt with the T-Register set to 102074.

9. When the parity bit test patterns have been loaded into memory the ground jumper should be removed and the Parity Error board replaced in slot A5 observing the same power precautions used in the above procedures. The top connector hood should be set to halt on detecting a parity error. Load 7033 into P-Register. Press PRESET, press RUN. The Computer should halt with the T-Register set to 0 and the PARITY light on.

10. Reverse the top connector hood so that the Computer will interrupt on detection of a parity error. Press the PRESET and RUN buttons. The next section of the diagnostic will test the Parity Error board's ability to interrupt on the detection of a parity error. The 0 (NOP) loaded into location 5 allows the Computer to return to the diagnostic routine without operator intervention. If the Computer fails to interrupt properly an error halt (HLT 21) is generated indicating a failure to interrupt.

11. DIAGNOSTIC TEST.

12. The diagnostic program performs the tests in sequential order. Each test assumes that the previous test was completed without failure. A list of the error halts and their descriptions is given in Table 1. By using the error halt description and the contents of the various registers it is possible in most cases to isolate the malfunction.

13. The diagnostic test checks the contents of the Parity Error Address Register. If the contents of this register do not compare with the stored address of the parity error a HLT 22 is generated, indicating a failure of the Parity Error Address circuitry.

14. The ability to turn the Parity Error circuitry on and off is tested by a programmed CLF 05 instruction to disable the Parity Error board. A parity error is then introduced. If the Parity Error board has failed to turn off, a parity error interrupt will be generated causing the test program to execute a HLT 23. Normal control operation will cause the diagnostic program to proceed to the next test.

15. The A and B Registers do not contain a parity bit and therefore parity errors detected during an addressable A or B Register function should be disregarded. Also during the memory write cycle there is no need to generate a parity error. If any occurred they should have been detected during the memory read cycle. The diagnostic program tests these conditions by addressing first the A and then the B Registers. Data is placed in the registers such that a

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Table 1. Diagnostic Halt Codes

HALT CODE	DESCRIPTION
102021	Did not interrupt on bad parity.
102022	Error address incorrect (Register contents not 7402).
102023	Control not cleared by CLF 5.
102024	Interrupted on (AAF + MWL) (Bad Parity)
102025	Interrupted on (BAF + MWL) (Bad Parity)
102026	Interrupted on (AAF) (Bad Parity)
102027	Interrupted on (BAF) (Bad Parity)
102030	Interrupted on (ISZ) (PH3) (AAF) (Bad Parity)
102031	Interrupted on (ISZ) (PH3) (BAF) (Bad Parity)
102032	Did not interrupt (ISZ) (PH3) ($\overline{AAF + BAF}$) (Bad Parity)
102033	Error address incorrect. Register contents not 11200 (if a 4K machine, register contents not 01200).
102034	Interrupted on (MWL) ($\overline{ISZ}$) (Bad Parity).
102035	Did not interrupt on ($\overline{MWL}$) (Bad Parity).
102036	Interrupted to I/O 10 after CLF 5 ($\overline{PRL5}$).
102037	Did not interrupt to I/O 10 after STF 5 (PRL5).
102040	Test sequence error - Reload program.
102044	Interrupt on good parity (A = Data B = Address)
102055	Did not interrupt on bad parity (A = Data B = Address)
102066	Error address incorrect (A = Error Address Register - B = Program Address)

parity error would normally be generated. If a parity error is generated during the execution of these functions or while the MWL (Memory Write Level) signal is true a HLT 24 or HLT 25 is generated. The next sequential test checks the A and B Addressable functions again, separately from the MWL signal. A failure of the A or B addressable functions will generate a HLT 26 or HLT 27 respectively.

16. The diagnostic program next checks the ISZ (Increment and Skip if Zero) instruction. This command is normally used as a memory reference instruction but when used with the A or B addressable registers could produce an incorrect parity error indication. Data containing parity errors is placed in the A and B Registers and then referenced by an ISZ instruction. The parity halt circuitry should inhibit parity error generation under these conditions. If it fails to do so a HLT 30 or HLT 31 is produced for the A and B functions respectively.

17. The ISZ instruction should be allowed to generate a parity error under normal memory reference conditions. The parity error should be generated during the Phase 3 machine cycle. The diagnostic first checks to see if the parity error is allowed to cause an interrupt and then checks to see that the parity error address is correct. Failure of one of these tests will cause the program to execute an error halt HLT 32 or HLT 33 respectively.

18. When the MWL signal is true and the ISZ signal is false a parity error should not be allowed to cause an interrupt or halt Computer operation. The diagnostic tests this function and on failure generates a HLT 34. Next the MWL signal is tested alone. When the MWL signal is false the Computer should interrupt on detection of a parity error. If the Computer fails to do so an error halt HLT 35 is generated.

19. The ability of the Parity Error board to hold off interrupts while processing a parity error is tested by inducing a parity error and then causing an interrupt from I/O slot 10. If the test fails then the PRL5 (Priority Low) signal did not drop inhibiting lower priority devices from interrupting. A failure of this test produces an error halt HLT 36. The CLC 00 instruction should clear the parity error indication causing the PRL5 signal to go true. The STF 00 instruction turns the interrupt system back on. If the induced interrupt from I/O slot 10 does not occur after the parity error indication has been cleared an error halt HLT 37 is generated.

20. Error halt HLT 40 provides for errors in the program procedure or test sequence. The diagnostic procedure should be repeated from the beginning as well as reloading the diagnostic program.

21. The Parity Calculating Network is checked by using a series of data patterns which exercise differ-

ent parity configurations. By observing the data or address that generated a failure the group of gates responsible can be isolated. A parity error interrupt that is generated by correct data will cause an error halt HLT 44. A failure to interrupt on incorrect data will cause an error halt HLT 55.

22. When a parity error occurs the address of the error is stored in the Parity Error Address Register on the Parity Error board. When the artificial parity errors are tested the program compares the address read out of the Parity Error Address Register with the actual address of the parity error. If the two disagree an error halt HLT 66 is generated.

23. When an error halt HLT 44, HLT 55, or HLT 66 occurs the contents of the A and B Registers (Error Address Register and parity error address respectively) can be displayed by single cycling twice and viewing the Switch Register (first the B and then the A Register is displayed). After successful completion of the diagnostic the program corrects the test parity data in memory. The Computer should then execute a normal HLT 77 (102077 octal).

24. To order a replacement tape, address the order or inquiry to your local Hewlett-Packard field office. See the list at rear of the Memory Parity Check operating manual for field-office addresses.

```
0001                    ASMB,A,B,L,T          2-4-69 ERH
BX          007344
DMP         001057
EHR         000047
FIX         007333
FPE         001051
K2          001035
K3          001036
K4          001037
K5          001040
MIK         007345
NDT         001100
PE9         001043
RPE         001062
RRR         000050
T1          007112
T10         007236
T11         007255
T12         007302
T13         007311
T14         007320
T2          007126
T3          007134
T4          007143
T5          007160
T6          007172
T7          007177
T8          007206
T9          007225
ADDR        001047
BADP        007251
BKT14       007327
BKTP        000042
CLEAN       007346
EH21        001000
EH22        001001
EH23        001002
EH24        001003
EH25        001004
EH26        001005
EH27        001006
EH30        001007
EH31        001010
EH32        001011
EH33        001012
EH34        001013
EH35        001014
EH36        001015
EH37        001016
EH40        001017
EH44        001020
EH55        001021
EH66        001022
FORK        001050
FOUR        001034
IBZA1       001025
JMPBK       001026
```

```
K3.9      001041
K5.9      001042
K7401     000041
K7404     001023
MASK1     001024
MASK2     001027
PE10      001045
PE12      001046
PESU      007000
PICUP     000051
PTRN1     001030
PTRN2     001031
PTRN3     001032
THREE     001033
** NO ERRORS*
```

```
0001                    ASM8,A,B,L,T        2-4-69 ERH
0002*
0003*  PARITY ERROR DIAGNOSTIC FOR 12580B
0004*                              12598A
0005*
0006*  TEST PROCEDURE
0007*
0008*    A BOARD WITH STANDARD INTERRUPT CIRCUITRY MUST BE IN I/O 10.
0009*
0010*    ---TURN OFF POWER BEFORE REMOVING OR INSERTING BOARD---
0011*    1. PLUG PEI BOARD IN A5 - INSTALL HOOD IN INTERRUPT MODE.
0012*    2. LOAD 0 IN ADDRESS 5.
0013*    3. LOAD PROGRAM.
0014*    4. REMOVE PEI BOARD. IF 4K MACHINE, SET SWITCH 15.
0015*    5. PRESET, SA 7000 OCTAL, RUN.
0016*         (SHOULD HALT T = 102072 OCTAL).
0017*    6. GROUND PIN 52 OF A5. IF 4K MACHINE, SET SW.REG. BIT 15.
0018*    7. RUN!  (SHOULD HALT T = 102074 OCTAL).
0019*    8. REPLACE PEI BOARD IN A5 - PUT HOOD IN PARITY HALT MODE.
0020*       -REMOVE GROUND FROM PIN 52 OF A5-.
0021*    9. PRESET, RUN (SHOULD HALT T = 0, PARITY LIGHT ON.)
0022*   10. TURN HOOD TO INTERRUPT MODE.
0023*   11. PRESET, RUN (SHOULD HALT T = 102077 OCTAL)
0024*
0025*  ERROR HALTS
0026*
0027*    HALT 21    DID NOT INTERRUPT ON BAD PARITY
0028*    HALT 22    ERROR ADDRESS INCORRECT (REGISTER CONTENTS NOT 7402)
0029*    HALT 23    CONTROL NOT CLEARED BY CLF 5
0030*    HALT 24    INTERRUPTED ON (AAF TRUE + MWL TRUE)(BAD PARITY)
0031*    HALT 25    INTERRUPTED ON (BAF TRUE + MWL TRUE)(BAD PARITY)
0032*    HALT 26    INTERRUPTED ON (AAF)(BAD PARITY).
0033*    HALT 27    INTERRUPTED ON (BAF)(BAD PARITY).
0034*    HALT 30    INTERRUPTED ON (ISZ)(PH3)(AAF)(BAD PARITY)
0035*    HALT 31    INTERRUPTED ON (ISZ)(PH3)(BAF)(BAD PARITY)
0036*    HALT 32    DID NOT INTERRUPT (ISZ)(PH3)(BAD PARITY)
0037*    HALT 33    ERROR ADDRESS INCORRECT - REG. CONTENTS NOT 11200.
0038*                 (SHOULD BE 1200 ON 4K MACHINE).
0039*    HALT 34    INTERRUPT ON (MWL)(ISZ NOT)(BAD PARITY)
0040*    HALT 35    DID NOT INTERRUPT (MWL NOT)(BAD PARITY)
0041*    HALT 36    INTERRUPT TO I/O 10 AFTER CLF 5 (PRL5 NOT)
0042*    HALT 37    FAILURE TO INTERRUPT TO I/O 10 AFTER STF 5.
0043*    HALT 40    TEST SEQUENCE ERROR - RELOAD PROGRAM!
0044*    HALT 44    INTERRUPTED ON GOOD PARITY
0045*                 (A = DATA  B = ADDR.)
0046*    HALT 55    FAILURE TO INTERRUPT ON BAD PARITY
0047*                 (A = DATA  B = ADDR.)
0048*    HALT 66    ERROR ADDRESS REGISTER DOES NOT AGREE
0049*                 WITH PROGRAM ADDRESS.
0050*                 (A = ADDRESS REG. B = PROGRAM ADDRESS)
0051*       --AFTER ERROR HALTS 44, 55, & 66, B & A REGISTER
0052*         CONTENTS MAY BE OBSERVED BY SINGLE CYCLING TWICE
0053*         AND VIEWING IN THE SWITCH REGISTER (B THEN A)
0054*  PARITY ERROR HALT/INTERRUPT =
0055*                    (EAL PARITY)(MIC)(T3)((AAF NOT)(BAF NOT)(MWL) +
0056*                    (AAF NOT)(BAF NOT)(PH3)(ISZ))
0057*
```

```
0058*
0059*
0060*  TRAP  CELL  CONSTANTS
0061   00002                  ORG 2B
0062   00002 102002           HLT 2B       ERROR HLT
0063   00003 102003           HLT 3B
0064   00004 103004           HLT 4B,C        ERROR HALT
0065   00005 102005           HLT 5B       PE  TRAP CELL
0066   00006 102006           HLT 6B          ERROR HALT
0067   00007 102007           HLT 7B
0068   00010 102010           HLT 10B         INTR.
0069   00011 102011           HLT 11B
0070   00012 102012           HLT 12B              FROM
0071   00013 102013           HLT 13B
0072   00014 102014           HLT 14B                   SOME
0073   00015 102015           HLT 15B
0074   00016 102016           HLT 16B                       I/O
0075   00017 102017           HLT 17B
0076   00020 102020           HLT 20B                           DEVICE
0077*  INDIRECT ADDRESS CONSTANTS
0078   00040                  ORG 40B
0079   00040 007112           DEF T1
0080   00041 007401  K7401     OCT 7401
0081   00042 007160  BKTP     DEF T5
0082   00043 007172           DEF T6
0083   00044 007225           DEF T9
0084   00045 007255           DEF T11
0085   00046 007302           DEF T12
0086   00047 015051  EHR      JSB FPE         LINK TO PE ROUTINE
0087   00050 015062  RRR      JSB RPE         LINK TO RECOVER R.
0088   00051 114040  PICUP    JSB 40B,I
0089*  ERROR HALTS
0090   01000                  ORG 1000B
0091   01000 102021  EH21     HLT 21B
0092   01001 102022  EH22     HLT 22B
0093   01002 102023  EH23     HLT 23B
0094   01003 102024  EH24     HLT 24B
0095   01004 102025  EH25     HLT 25B
0096   01005 102026  EH26     HLT 26B
0097   01006 102027  EH27     HLT 27B
0098   01007 102030  EH30     HLT 30B
0099   01010 102031  EH31     HLT 31B
0100   01011 102032  EH32     HLT 32B
0101   01012 102033  EH33     HLT 33B
0102   01013 102034  EH34     HLT 34B
0103   01014 102035  EH35     HLT 35B
0104   01015 102036  EH36     HLT 36B
0105   01016 102037  EH37     HLT 37B
0106   01017 102040  EH40     HLT 40B
0107   01020 102044  EH44     HLT 44B
0108   01021 102055  EH55     HLT 55B
0109   01022 102066  EH66     HLT 66B
0110*  CONSTANTS
0111   01023 007404  K7404     OCT 7404
0112   01024 107402  MASK1    OCT 107402
0113   01025 037400  ISZA1    OCT 37400       (ISZ 1400)
0114   01026 124042  JMPBK    JMP BKTP,I      JUMP BACK TO PROGRAM
```

```
0115  01027 017777  MASK2  OCT  17777
0116  01030 007400  PTRN1  OCT  7400
0117  01031 170526  PTRN2  OCT  170526     ODD PARITY PATTERN
0118  01032 015705  PTRN3  OCT  015705     EVEN PARITY PATTERN
0119  01033 000003  THREE  OCT   3
0120  01034 000004  FOUR   OCT  4
0121  01035 002000  K2     OCT   2000
0122  01036 003000  K3     OCT   3000
0123  01037 004000  K4     OCT  4000
0124  01040 005000  K5     OCT  5000
0125  01041 003777  K3.9   OCT   3777
0126  01042 005777  K5.9   OCT   5777
0127  01043 011200  PES    OCT  1120
0128  01044 011200         OCT  1120
0129  01045 000000  PE10   OCT   0
0130  01046 000000  PE12   OCT   0
0131  01047 011200  ADDR   OCT  1120
0132  01050 001200  FORK   OCT  1200
0133*  FAIL ROUTINE
0134  01051 000000  FPE    NOP
0135  01052 102044         HLT   44B       B=ADDR, A=DATA
0136  01053 106601         OTB  1          ADDRESS
0137  01054 102601         OTA  1          DATA
0138  01055 071057         STA   DMP       TREE CHECK
0139  01056 125051         JMP  FPE,I      RETURN
0140  01057 000000  DMP    NOP
0141*  RECOVER ROUTINE
0142  01060 007326         DEF  BKT14-1
0143  01061 007327         DEF  BKT14
0144  01062 000000  RPE    NOP
0145  01063 102505         LIA  5B         GET REG.
0146  01064 011027         ANL  MASK2      REMOVE BIT 15
0147  01065 050001         CPA  1B         REG=ADDR.
0148  01066 002001         RSS             YES
0149  01067 102066         HLT  66B        NO-REG=A, ADDR=B
0150  01070 106601         OTB  1          ADDRESS
0151  01071 102601         OTA  1          REG. CONT.
0152  01072 061062         LDA  RPE
0153  01073 051060         CPA  RPE-2     DID WE COME FROM TEST 14?
0154  01074 125061         JMP  RPE-1,I    YES GO BACK
0155  01075 102601         OTA  1          NO!  SW. REG. = LOCATION OF BAD
0156  01076 102040         HLT  40B        CAME FROM WRONG PLACE
0157  01077 025076         JMP  *-1
0158*  FAIL TO DET PE
0159  01100 000000  NDT    NOP
0160  01101 102055         HLT  55B        B=ADDR, A=DATA
0161  01102 106601         OTB  1          ADDRESS
0162  01103 102601         OTA  1          DATA
0163  01104 071057         STA  DMP        TREE CHECK
0164  01105 125100         JMP  NDT,I
0165*
0166*  SET UP PARITY ERRORS IN MEMORY
0167*
0168*              *****REMOVE  PE  BOARD*****
0169*
 170  07000                ORG  7000B
 171  07000 061031  PESU   LDA  PTRN2
```

```
0172  07001 065035          LDB K2
0173  07002 017333          JSB FIX         SET UP PB=0, ODD PTRN.
0174  07003 061032          LDA PTRN3
0175  07004 065040          LDB K5
0176  07005 017333          JSB FIX         SET UP PB=0, EVEN PTRN.
0177  07006 002400          CLA
0178  07007 071045          STA PE10        FIX
0179  07010 071046          STA PE12          BAD
0180  07011 171044          STA PE9+1,I         PARITY
0181  07012 073400          STA 7400B
0182  07013 073401          STA 7401B
0183  07014 073402          STA 7402B
0184  07015 063251          LDA BADP                PARITY ISTR.
0185  07016 102072          HLT 72B
0186*
0187*              *****PUT GND ON PIN 52*****
0188*
0189  07017 102501          LIA 1
0190  07020 002021          SSA,RSS         CHANGE ADDRESS
0191  07021 027024          JMP *+3           FOR 4K
0192  07022 061050          LDA FORK            MACHINE..
0193  07023 071047          STA ADDR
0194  07024 061032          LDA PTRN3
0195  07025 065036          LDB K3
0196  07026 017333          JSB FIX         SET UP PB=1,EVEN PTRN.
0197  07027 061031          LDA PTRN2
0198  07030 065037          LDB K4
0199  07031 017333          JSB FIX         SET UP PB=1, ODD PTRN.
0200  07032 102074          HLT 74B
0201*
0202*              ***** PLUG IN BOARD *****
0203*
0204  07033 027100          JMP 7100B    BEGIN TESTS
0205  07100                 ORG 7100B
0206  07100 063400          LDA 7400B
0207  07101 000000          NOP
0208  07102 000000          NOP
0209  07103 000000          NOP
0210*  TEST THAT IT IS POSSIBLE TO INTERRUPT
0211  07104 002400          CLA
0212  07105 071400          STA 1400B
0213  07106 102105          STF 5B
0214  07107 060051          LDA PICUP
0215  07110 070005          STA 5B        SET UP RETURN
0216  07111 027402          JMP 7402B
0217  07112 000000    I1    NOP
0218  07113 102505          LIA 5B
0219  07114 103105          CLF 5B
0220  07115 102601          UTA 01      REG. CONTENTS
0221  07116 051024          LPA MASK1   DID WE COME FROM 7402
0222  07117 002001          RSS
0223  07120 102022          HLT 22B       NO! ERROR HALT
0224  07121 064000          LDB 0
0225  07122 053112          LDA I1
0226  07123 051023          LPA K7400     CHECK VALUE OF P
0227  07124 002001          RSS
0228  07125 102021          HLT 21B     NO  NOT FROM 7402
```

```
0229*  TEST THAT CAN TURN CONTROL OFF
0230   07126 103105  T2     CLF 5B
0231   07127 061002         LDA EH23
0232   07130 070005         STA 5B          SET UP EH
0233   07131 103105         CLF 5B          READY
0234   07132 160041         LDA K7401,I
0235   07133 000000         NOP
0236*  CHECK ADDR. A & B
0237   07134 061003  T3     LDA EH24
0238   07135 070005         STA 5B          SET UP EH
0239   07136 002400         CLA
0240   07137 102105         STF 5B          READY -
0241   07140 064000         LDB 0           TEST
0242   07141 000000         NOP
0243   07142 103105         CLF 5B          INTERRUPT OFF...
0244   07143 061004  T4     LDA EH25
0245   07144 070005         STA 5B          SET EH
0246   07145 006400         CLB
0247   07146 102105         STF 5B          READY -
0248   07147 060001         LDA 1B          TEST
0249   07150 000000         NOP
0250   07151 103105         CLF 5B          INTERRUPT OFF...
0251*  CHECK ADDR. A & B ISZ
0252   07152 061005         LDA EH26
0253   07153 070005         STA 5B          SET EH
0254   07154 061025         LDA ISZA1       SET UP INST.
0255   07155 065026         LDB JMPBK       SET UP RETURN
0256   07156 102105         STF 5B          READY -
0257   07157 024000         JMP 0           TEST
0258   07160 000000  T5     NOP
0259   07161 103105         CLF 5B          INTERRUPT OFF...
0260   07162 061006         LDA EH27
0261   07163 070005         STA 5B          SET EH
0262   07164 065025         LDB ISZA1       SET UP INSTR.
0263   07165 061026         LDA JMPBK
0264   07166 002004         INA
0265   07167 070002         STA 2B          SET UP RETURN
0266   07170 102105         STF 5B          READY -
0267   07171 024001         JMP 1           TEST
0268   07172 000000  T6     NOP
0269   07173 103105         CLF 5B          INTERRUPT OFF...
0270   07174 003400         CCA
0271   07175 040003         ADA 3B
0272   07176 070002         STA 2B          RETURN LOC. 2 TO HLT 2
0273*  CHECK ADDR. A & B ISZ PH 3
0274   07177 061007  T7     LDA EH30
0275   07200 070005         STA 5B          SET EH
0276   07201 002400         CLA
0277   07202 102105         STF 5B          READY -
0278   07203 034000         ISZ 0           TEST
0279   07204 000000         NOP
0280   07205 103105         CLF 5B          INTERRUPT OFF...
0281   07206 061010  T8     LDA EH31
0282   07207 070005         STA 5B          SET EH
0283   07210 006400         CLB
0284   07211 102105         STF 5B          READY -
0285   07212 034001         ISZ 1           TEST
```

```
0286  07213 000000          NOP
0287  07214 103105          CLF 5B          INTERRUPT OFF...
0288*  TEST  ISZ  PHASE 3
0289  07215 061026          LDA JMPBK
0290  07216 002004          INA
0291  07217 002004          INA
0292  07220 070005          STA 5B          SET UP RETURN
0293  07221 102105          STF 5B          READY -
0294  07222 135043          ISZ PE9,I
0295  07223 000000          NOP
0296  07224 102032          HLT 32B         ERROR HALT
0297  07225 102505  T9      LIA 5B
0298  07226 103105          CLF 5B          INTERRUPT OFF...
0299  07227 011027          ANL MASK2
0300  07230 065047          LDB ADDR      GET CORRECT ADDR.
0301  07231 051047          CPA ADDR      CHECK REG.
0302  07232 002001          RSS
0303  07233 102033          HLT 33B         ERROR HALT - REG. WRONG
0304  07234 106601          OTB 01        ADDR
0305  07235 102601          OTA 01        REG.  CONTENTS
0306*  CHECK STORE
0307  07236 061013  T10     LDA EH34
0308  07237 070005          STA 5B          SET EH
0309  07240 002400          CLA
0310  07241 102105          STF 5B          READY -
0311  07242 071045          STA PE10        TEST
0312  07243 000000          NOP
0313  07244 103105          CLF 5B          INTERRUPT OFF...
0314*  CHECK ISZ  PHASE 1
0315  07245 061026          LDA JMPBK
0316  07246 041033          ADA THREE
0317  07247 070005          STA 5B          SET UP RETURN
0318  07250 102105          STF 5B          READY -
0319  07251 035500  BADP    ISZ 1500H
0320  07252 000000          NOP
0321  07253 000000          NOP
0322  07254 102035          HLT 35B         ERROR HALT
0323  07255 103105  T11     CLF 5B    INTR. OFF
0324*  CHECK  PRIORITY CHAIN
0325  07256 061015          LDA EH36
0326  07257 070010          STA 10B
0327  07260 002400          CLA
0328  07261 070005          STA 5B
0329  07262 102105          STF 5B
0330  07263 061046          LDA PE12
0331  07264 000000          NOP
0332  07265 000000          NOP
0333  07266 106700          CLC 0     CLEAR ALL CONTROLS
0334  07267 102710          STC 10B   TURN ON I/O 10
0335  07270 102110          STF 10B   SET FLAG 10
0336  07271 102100          STF 0     TURN INTR SYST ON
0337  07272 000000          NOP       FAIL TEST IF INTR TO 10
0338  07273 061026          LDA JMPBK
0339  07274 041034          ADA FOUR
0340  07275 070010          STA 10B   SET UP RETURN
0341  07276 102105          STF 5B
0342  07277 000000          NOP       TEST IF CAN INTR TO 10
```

```
0343   07300 000000          NOP
0344   07301 102037          HLT 37B         ERROR HALT
0345   07302 003400   T12    CCA
0346   07303 107700          CLC 0,C  TURN INTR SYSTEM  OFF
0347   07304 040011          ADA 11B
0348   07305 070010          STA 10B  FIX   TRAP CELL UP
0349*   CHECK PARITY TREE    (GOOD PARITY)
0350   07306 060047          LDA EHR
0351   07307 070005          STA 5B          SET PE FAIL LINK
0352   07310 065035          LDB K2          SET START ADDR.
0353   07311 102105   T13    STF 5B   READY
0354   07312 160001          LDA 1,I         TEST
0355   07313 000000          NOP
0356   07314 055041          CPB K3,9        DONE ?
0357   07315 027320          JMP T14         YES- GO TO TEST 14
0358   07316 006004          INB             NO
0359   07317 027311          JMP T13             GO BACK
0360*   CHECK PARITY TREE   (BAD PARITY)
0361   07320 060050   T14    LDA ERR
0362   07321 070005          STA 5B          SET PE RECOVER LINK
0363   07322 065037          LDB K4          SET START ADDR.
0364   07323 102105          STF 5B          READY -
0365   07324 160001          LDA 1,I         TEST
0366   07325 000000          NOP
0367   07326 015100          JSB NOT
0368   07327 055042   BK114 CPB K5,9         DONE ?
0369   07330 027346          JMP CLEAN       YES- GO TO CLEAN UP
0370   07331 006004          INB             NO
0371   07332 027323          JMP T14+A           GO BACK
0372*   PARITY ERROR FIX ROUTINE
0373   07333 000000   FIX    NOP             PATTERN IN A
0374   07334 170001          STA 1,I         FIRST ADDR. IN B
0375   07335 001200          RAL             ROTATE PATTERN
0376   07336 006004          INB             NEXT ADDR.
0377   07337 037344          ISZ BX
0378   07340 027334          JMP FIX+1
0379   07341 063345          LDA MIK         FINISHED
0380   07342 073344          STA BX          INITALIZE COUNTER
0381   07343 127333          JMP FIX,I       RETURN TO PRG
0382   07344 177000   BX     OCT -1000       COUNTER
0383   07345 177000   MIK    OCT -1000
0384*   REMOVE ANY PARITY ERRORS FROM MEMORY
0385   07346 103105   CLEAN  CLF 5B   TURN OFF INTR.
0386   07347 006400          CLB
0387   07350 160001          LDA 1,I         CORRECT PARITY BIT
0388   07351 006004          INB             NEXT ADDRESS
0389   07352 055027          CPB MASK2       DONE ?
0390   07353 002001          RSS             YES
0391   07354 027350          JMP *-4         NO-LOOP BACK
0392   07355 003400          CCA
0393   07356 040006          ADA 6B
0394   07357 070005          STA 5B       FIX UP TRAP CELL
0395   07360 102105          STF 5B
0396   07361 102077          HLT 77B         DONE (AT LAST)
0397   07362 027000          JMP 7000B
0398   07400                 ORG 7400B
0399   07400 000000          OCT 0
```

```
0400   07401 000000          OCT 0
0401   07402 000000          OCT 0
0402   07403 000000          OCT 0
0403   07404 102021          HLT 21B
0404   07405 000000          OCT 0
0405                         END
** NO ERRORS*
```

UPDATING SUPPLEMENT 2 JULY 69

MANUAL IDENTIFICATION

Manual Serial Prefixed:

Manual Printed:

Manual Part Number:

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to correct manual errors (Errata) and to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Prefix-Serial	Changes
ALL	1,2

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes

CHANGE DESCRIPTION

1 Page DS-1, paragraph 5. Add the following note between paragraphs 5 and 6:

NOTE

An interface card with standard flag and interrupt circuitry must be installed in I/O slot 10 when this test is performed. The term ''standard'' refers to any interface card that interrupts when its flag and control FF's are set (provided that the interrupt system enable FF on the I/O control card is set). Typical examples of cards having standard interrupt circuitry are the buffered teleprinter interface card (HP part no. 02116-6168) and the punched tape reader interface card (HP part no. 02116-6002).

2 Page DS-1, paragraph 10. Insert after the second sentence: ''The Computer should halt with T = 102077 and the PARITY light on. This indicates the successful completion of this part of the test.

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12598A

MEMORY PARITY CHECK
(FOR 2114A AND 2114B COMPUTERS)

UPDATING SUPPLEMENT FOR OPERATING AND SERVICE MANUAL

21 APR 1970

MANUAL IDENTIFICATION

Manual Serial No. Prefix: N/A

Manual Printed: FEB 1969

Manual Part Number: 12598-9001

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Serial No. Prefix	Change

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes

Changes 1, 2, 3, and 4 dated 21 April 1970.

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CHANGE	DESCRIPTION
1	Page 1, title. Change the title to read: "MEMORY PARITY CHECK FOR THE 2114A AND 2114B COMPUTERS."
2	Page 1, paragraph 2. Change line 2 to read: ". . . 2114A and 2114B . . ."
3	Page 4, paragraph 21. a. Change line 9 to read: ". . .The Flag Flip-Flop is cleared via MC84D by . . ." b. Change line 31 to read: "the other input of MC92A true, setting the Flag Buffer."
4	Page 7/8, figure 3. Make the changes indicated in figure 1 of this supplement.

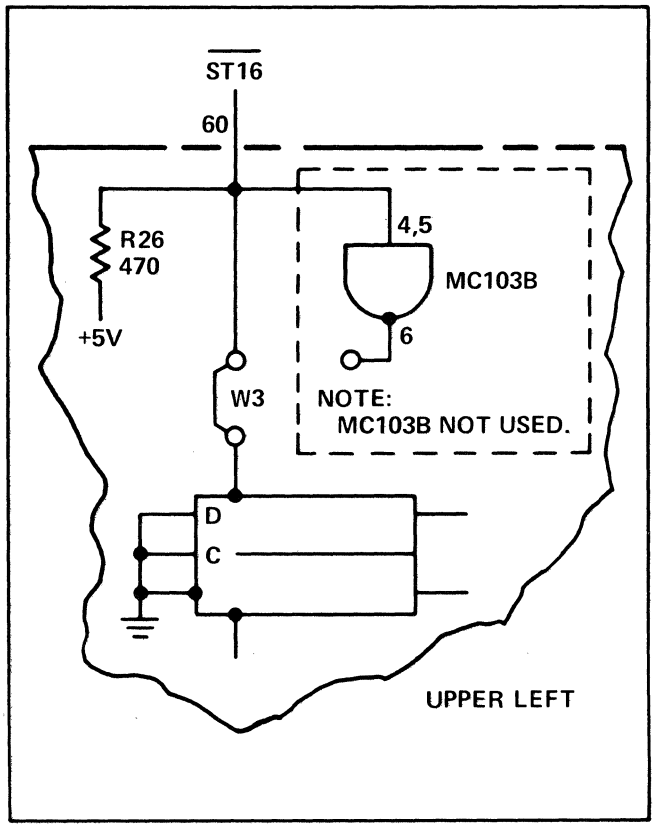

Figure 1. Parity Error Card (12598-6001), Partial Schematic Diagram Showing Errata Changes