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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

8001/8002A

μPROCESSOR LAB

INSTALLATION GUIDE

SERVICE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

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WARRANTY

The 8002A μProcessor Lab System (including options) is warranted against defective materials and workmanship under normal use and service for a period of 90 days from date of initial shipment. CRTs found to be defective within 12 months from the date of shipment will be exchanged at no charge (this does not include installation).

On site warranty repair is provided during normal working hours (for the 90-day period). Travel to the site is confined to those areas in which Tektronix states it has service facilities available for this product.

Tektronix shall be under no obligation to furnish warranty service if:

a. Attempts to install, repair, or service the equipment are made by personnel other than Tektronix service representatives.

b. Modifications are made to the hardware or software by personnel other than Tektronix service representatives.

c. Damage results from connecting the 8002A μProcessor Lab System to incompatible equipment.

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PREFACE

This manual provides information about installation, peripheral interfacing, and internal switch and jumper positions for the 8001/8002 μProcessor Lab. Use it as a reference source rather than as a text.

Throughout this manual, zeros are slashed where needed for clarity.

Schematic diagrams and specific information on the 8001/8002 μProcessor Lab may be found in the following service manuals.

8001/8002 μProcessor Lab 1702A PROM Programmer Service Manual

8001/8002 μProcessor Lab 2704/2708 PROM Programmer Service Manual

8001/8002 μProcessor Lab Real-Time Prototype Analyzer System Service Manual

8001/8002 μProcessor Lab System Service Manual

8001/8002 μProcessor Lab 8080 Emulator Processor Service Manual

8001/8002 μProcessor Lab 6800 Emulator Processor Service Manual

8001/8002 μProcessor Lab 9900 Emulator Processor Service Manual

8001/8002 μProcessor Lab Z80 Emulator Processor Service Manual

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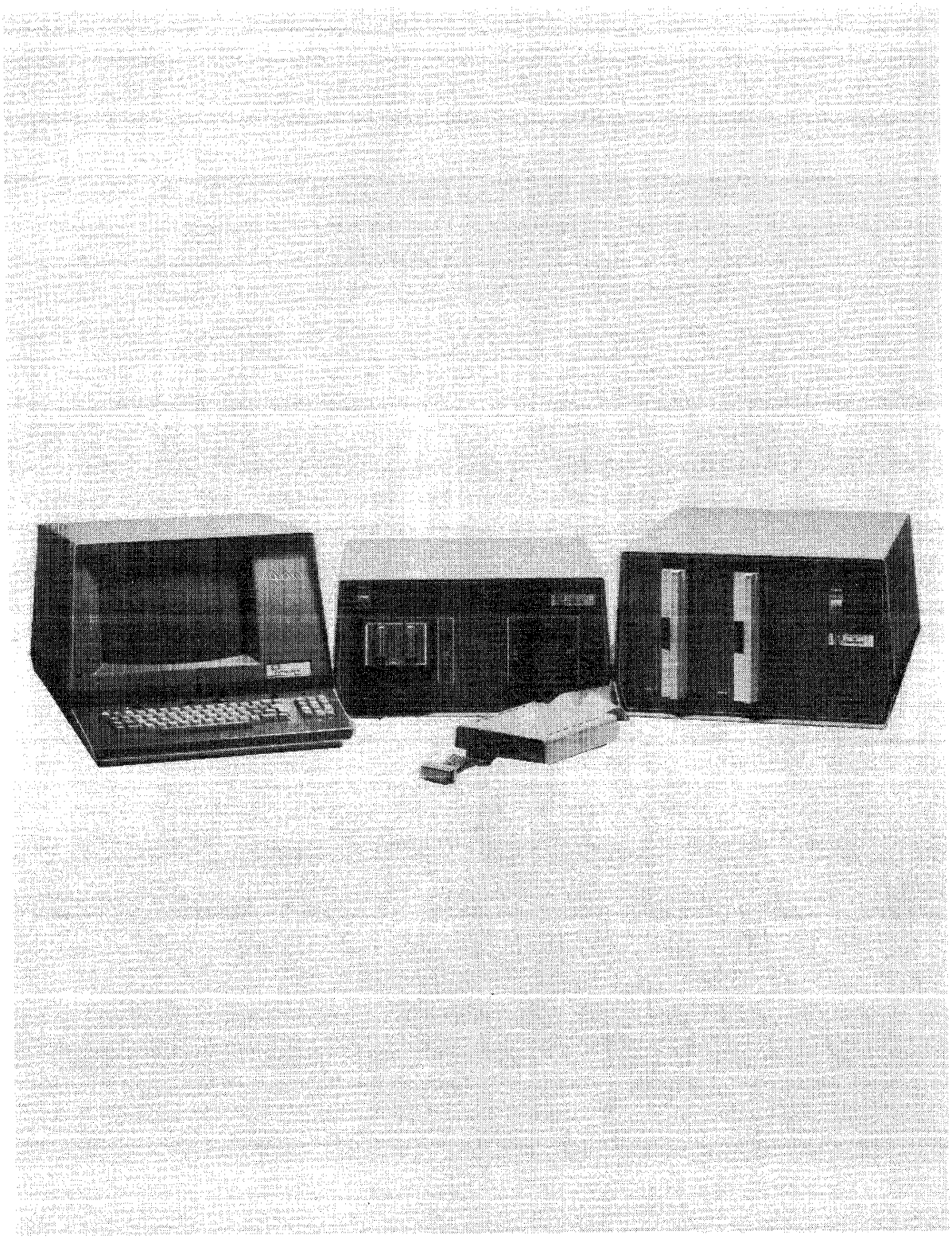

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8002 μProcessor Lab System.

Section 1

GENERAL INFORMATION

UNPACKING

The 8001/8002 μProcessor Lab and Flexible Disc Unit are shipped in separate cartons. Before unpacking these units, inspect each carton for signs of external damage. If any damage is detected, contact your nearest Tektronix representative.

Unpacking the 8001/8002 μProcessor Lab

To unpack the 8001/8002 μProcessor Lab, open the outer carton and remove the corner packing supports. Lift the inner carton and place on a flat surface. Remove the coiled power cord taped to the top of the inner carton and set it aside until the unit is to be connected to the primary power source. Open both ends of the inner carton and slide the μProcessor Lab out of the carton. Remove the plastic bag, cardboard packing, and front panel protective foam cushion from around the unit. The top cover is secured to the μProcessor Lab with three screws located along each side of the unit. Remove the screws and lift the top cover straight up. Set the cover aside. Remove the protective foam cushion on top of the modules (printed circuit boards).

Unpacking the Flexible Disc Unit

To unpack the Flexible Disc Unit, follow the same procedure for removing the outer carton, inner carton, and protective cushion as for the μProcessor Lab. Remove the three screws along each side and lift the top cover straight up. Set the cover aside. Visually inspect the inside of the unit for physical damage that may occur during shipping. Uncoil the Flexible Disc Unit interconnect cable and feed it through the channel opening provided in the rear panel. Replace the top cover on the Flexible Disc Unit.

Repacking for Shipment

If either the μProcessor Lab or Flexible Disc Unit is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner (with address), name of individual at your firm that can be contacted, complete serial number, and a description of the service required. If the original packaging is unfit for use or not available, repackage the equipment as follows:

1. Obtain a carton of corrugated cardboard having inside dimensions that are at least six inches more than the equipment dimensions, to allow for cushioning.

2. Surround the equipment with polyethylene sheeting to protect the finish.

3. Cushion the equipment on all sides with packing material or urethane foam between the carton and the sides of the equipment.

4. Seal with shipping tape or industrial stapler.

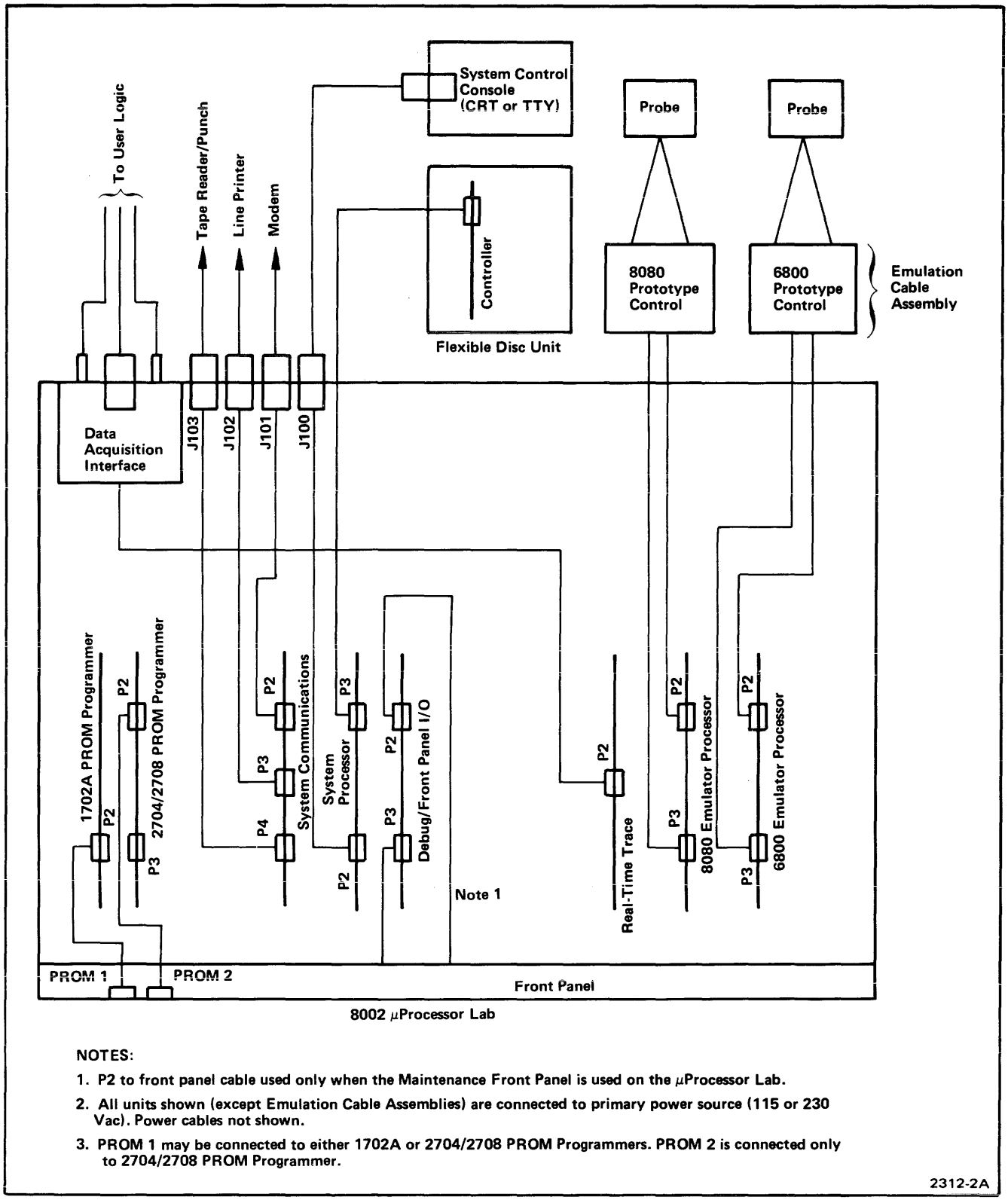
8001/8002 μPROCESSOR LAB INSTALLATION

The 8002 μProcessor Lab and Flexible Disc Unit should be installed and operated on a flat surface. The units should be close enough to each other for the interconnecting cables to reach. Both units draw cooling air through openings in the bottom of the cabinets. The air is expelled out the back by two fans. These units should not be located where paper, plastic, carpeting, or other materials might block the air intakes and cause overheating. Allow at least four inches clearance behind the units so the air flow is not restricted.

The 8001 μProcessor Lab installation requirements are the same as for 8002 μProcessor Lab.

Cable Interconnections

Refer to Fig. 1-1 for the 8001/8002 μProcessor Lab System interconnect diagram. Connect the cables as follows:



NOTES:

1. P2 to front panel cable used only when the Maintenance Front Panel is used on the μProcessor Lab.
2. All units shown (except Emulation Cable Assemblies) are connected to primary power source (115 or 230 Vac). Power cables not shown.
3. PROM 1 may be connected to either 1702A or 2704/2708 PROM Programmers. PROM 2 is connected only to 2704/2708 PROM Programmer.

2312-2A

Fig. 1-1. 8001/8002 μProcessor Lab System Interconnect Diagram.

1. Route the interconnecting ribbon cable from the rear of the Flexible Disc Unit through the center cableway located on the power supply cover on the back panel of the 8002 μProcessor Lab. The cable should be gripped between the metal grounding bars of the cable clamp assembly. Make sure the bared ground plane of the ribbon cable is making contact with the cable clamps to ensure a good ground connection. Connect P3 of the cable to the board edge connector, labeled P3, of the System Processor module. Replace the top cover on the μProcessor Lab.

2. Connections and routing for interconnecting cables to optional or peripheral equipment must be accomplished in accordance with Fig. 1-1 and instructions in the individual equipment manuals. The emulation cable assemblies that enter the center and right cableways (from a front panel view) on the back panel of the μProcessor Lab must be correctly installed in the cable clamps. Make sure the bared ground plane of the ribbon cables are making contact with the cable clamps to ensure a good ground connection.

3. Auxiliary bus and ground connections on terminal block TB2, located on the back panel of the μProcessor Lab, provide access to an auxiliary power bus, logic or common ground, and chassis ground. Connections are as follows:

TB2-1 to auxiliary power bus lines on the motherboard.

TB2-2 to logic ground bus lines on the motherboard.

TB2-3 to chassis ground.

NOTE

A shorting strap is installed between TB2-2 and TB2-3 to provide a single common tie point between logic (common) ground and chassis ground (earth). In the event the shorting strap is removed, a one megohm bleeder resistor between TB2-2 and TB2-3, ensures a limited potential difference between logic and chassis ground.

GROUNDING

The installation of a proper ground system for the overall μProcessor Lab System (including any optional and peripheral equipment) is extremely important. The following grounding procedures are recommended to provide a proper ground system.

1. Make sure the primary power cords of all units (including the user's prototype equipment) are connected to outlets that are on the same ground system.

2. If the 8002 μProcessor Lab System (including the user's prototype equipment(is operated in a high static environment, use a grounding strap that is as short as possible between the μProcessor Lab and Flexible Disc Unit. Use copper braid strap or other low impedance wire, with soldered terminal lugs, for the grounding straps.

3. Attach grounding strap lugs to the chassis of the units. Ensure lugs make good contact with bare metal by removing paint or protective coating from the metal before attaching grounding lug.

When the 8001/8002 μProcessor Lab System is being used with an oscilloscope or other test equipment during In-prototype testing, proper grounding will eliminate ground loops and reduce susceptibility to static discharge.

A grounding strap between the μProcessor Lab chassis and the oscilloscope chassis is necessary to prevent static discharge. The oscilloscope, when connected to the trigger from the Data Acquisition Interface unit, establishes a second tie point between the logic and chassis ground of the μProcessor Lab. To prevent ground loops when the oscilloscope is connected, remove the strap between TB2-2 and TB2-3 on the back panel of the μProcessor Lab. This establishes the common tie point between logic and chassis ground at the oscilloscope, not at both units.

Any unused leads of the P6451 Logic Probes should be grounded or, if the probe is not in use, disconnect it from the Data Acquistition Interface unit.

POWER SOURCE

CAUTION

The μProcessor Lab and Flexible Disc Unit are both designed to be operated from a single-phase power source that has one of its current-carrying conductors (neutral) at ground (earth) potential. Operating from power sources where both current-carrying conductors are isolated or above ground potential (such as phase-to-phase on a multiphase system, or across the legs of a 110-220 volt single-phase, three-wire system) is not recommended, since only the line conductor has over-current (fuse) protection within the unit.

The ac power connector is a three-wire polarized plug with the ground (earth) lead connected directly to the instrument frame to provide electric shock protection. Connect this plug only to a three-wire outlet which has an earth ground. If the unit is connected to any other power source, the unit frames must be connected to an earth ground system.

The μProcessor Lab and Flexible Disc Unit are both designed to operate from a 115-230 volt nominal line voltage that has a frequency of 50-60 Hz. The Flexible Disc Unit is factory wired for 115 volts, 60 Hz operation; however, 230 volts, 50 Hz configuration is available by special order. Each unit has a separate power cord and requires a separate outlet for the primary power. The system power requirements are as follows:

8002 μProcessor Lab	3.5 amps at 115 V, ±10%, 60 Hz 2.0 amps at 230 V, ±10%, 50 Hz
Flexible Disc Unit	3.0 amps at 115 V, ± 10%, 60 Hz 1.5 amps at 230 V, ± 10%, 50 Hz

NOTE

The Flexible Disc Unit has a warning sign above the primary input power jack stating the unit is wired for a specific voltage and frequency at the factory.

The system fusing requirements for 115 volt or 230 volt primary power sources are as follows:

	AMP	VOLTS
8002 μProcessor Lab		
Primary (F4)	6 A	115 V
	3 A	230 V
± 12 Vdc Supply (F3)	2 A	115 V
	1 A	230 V
Flexible Disc Unit		
Primary (F1)	4 A	115 V
	2 A	230 V
Disc Drive (F3)	2.5 A	115 V
	1.5 A	230 V

WARNING

Dangerous voltages exist several places inside the units. Disconnect the μProcessor Lab and Flexible Disc Unit from the power source before removing or replacing the top cover. Only qualified technical personnel should attempt to change the power supply jumper arrangement. Unfamiliarity with electronic equipment and safety procedures can result in personal injury.

STATIC PRECAUTIONS

CAUTION

Static discharge can damage many semiconductor components used in these assemblies.

Many semiconductor components, especially MOS type components, can be damaged by static discharge. Damage may not be catastrophic, therefore, not immediately apparent. It usually appears as a "weakening" of the semiconductor characteristics. Devices that are particularly susceptible are: MOS, CMOS, JFETs, and high impedance OP amps. Damage can be significantly reduced by observing the following precautions:

1. Minimize handling by keeping assemblies, modules, or components in their original containers until ready for use. Minimize the removal and installation of semiconductors from their circuit boards.

2. Observe precautionary measures to reduce or eliminate static discharge when handling static sensitive devices or circuit assemblies, by grounding yourself on the instrument chassis when installing or removing an assembly with semiconductor components.

3. Hold the assembly or device by its sides rather than touching semiconductor terminals or conductive lines to these terminals.

4. All test equipment, accessories, and soldering tools should be connected to earth ground.

5. Use containers made of conductive material or filled with conductive material for storage and transportation. Avoid using ordinary plastic containers. Any static sensitive part or assembly (circuit board) that is to be returned to Tektronix, Inc. should be packaged in its original container or one with anti-static packaging material.

MODULE INSTALLATION

CAUTION

Before installing or removing a module, switch the POWER to the μProcessor Lab OFF.

NOTE

The red wire on each cable designates the side of the cable plug that is connected to pin 1 in the mating connector. In the μProcessor Lab, pin 1 of the mating connector on the module is always located toward the rear of the unit.

The module card connector is offset to ensure that the module cannot be plugged in backwards. After the module has been correctly positioned, press down firmly on the two plastic lifters (at the board edge) until the 100 pin edge connector (P1) snaps into place.

The recommended arrangement for the modules (printed circuit boards) is shown in Fig. 1-2. The modules may be arranged in other configurations if the following guidelines are not violated:

1. Positions 1 and 2	PROM Programmer modules may be located in either of these positions. (2 positions)
2. Positions 3 thru 8	The system modules may be located in any position within this section. (6 positions)
3. Position 9	Debug/Front Panel module. (1 position)
4. Positions 10 thru 20	The program modules may be located in any positions within this section. (11 positions)

NOTE

The location of a module within a section may be limited by the length of interconnecting cables.

Due to power supply limitations, no more than two emulator processor modules should be installed in a 8001/8002 μProcessor Lab configured for 60 Hz operation. No more than one emulator processor module should be installed in a 8001/8002 μProcessor Lab configured for 50 Hz operation (special order).

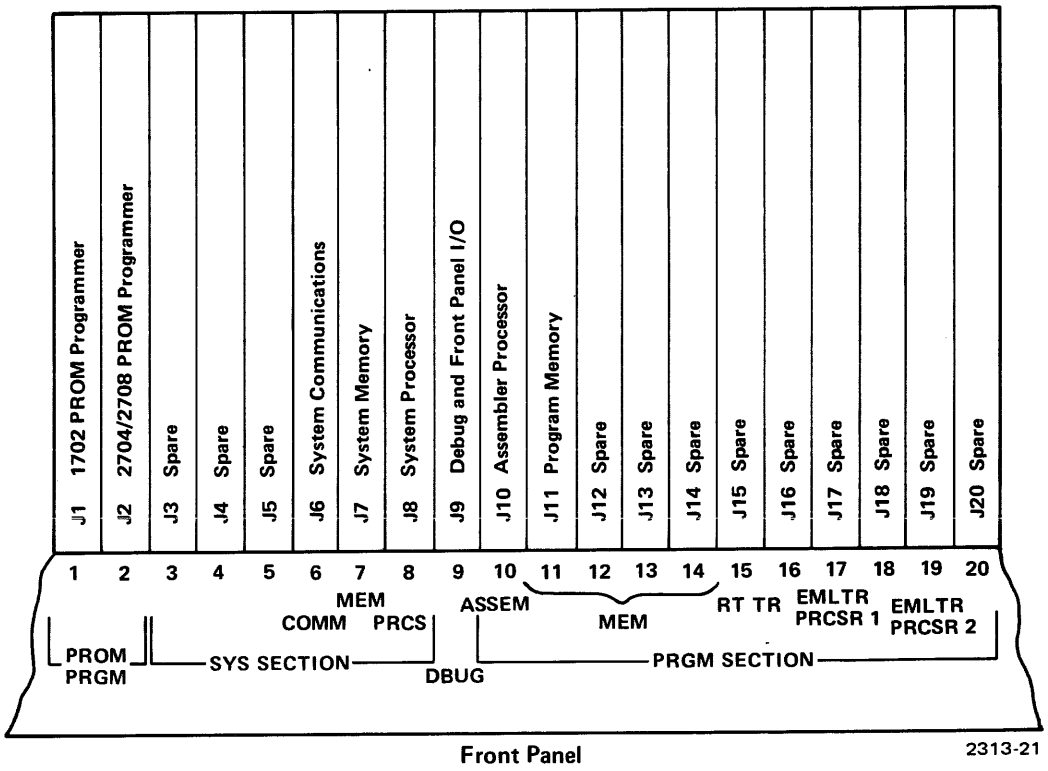


Fig. 1-2. 8001/8002 μProcessor Lab Module Arrangement.

The ribbon cables and connectors within the μProcessor Lab are installed prior to shipping. Make sure each connector is properly seated. Fig. 1-2 illustrates the correct location for each connector on the modules. Visually inspect the inside of the unit for physical damage that may have occurred during shipping. Do not replace the top cover on the μProcessor Lab at this time.

MODULE COMPONENT NAMING

The module card is divided into a grid of rows and columns (see Fig. 1-3) to locate components. The component name is determined by the location of the component on the module. The component name consists of four parts. The first part is a letter designating the type of component. The next is a single digit indicating the row and then two digits indicating the column of the component. Finally a digit ranging from 0 to 9 indicates where the component is located between two columns.

CIRCUIT NUMBER LOCATION GUIDE

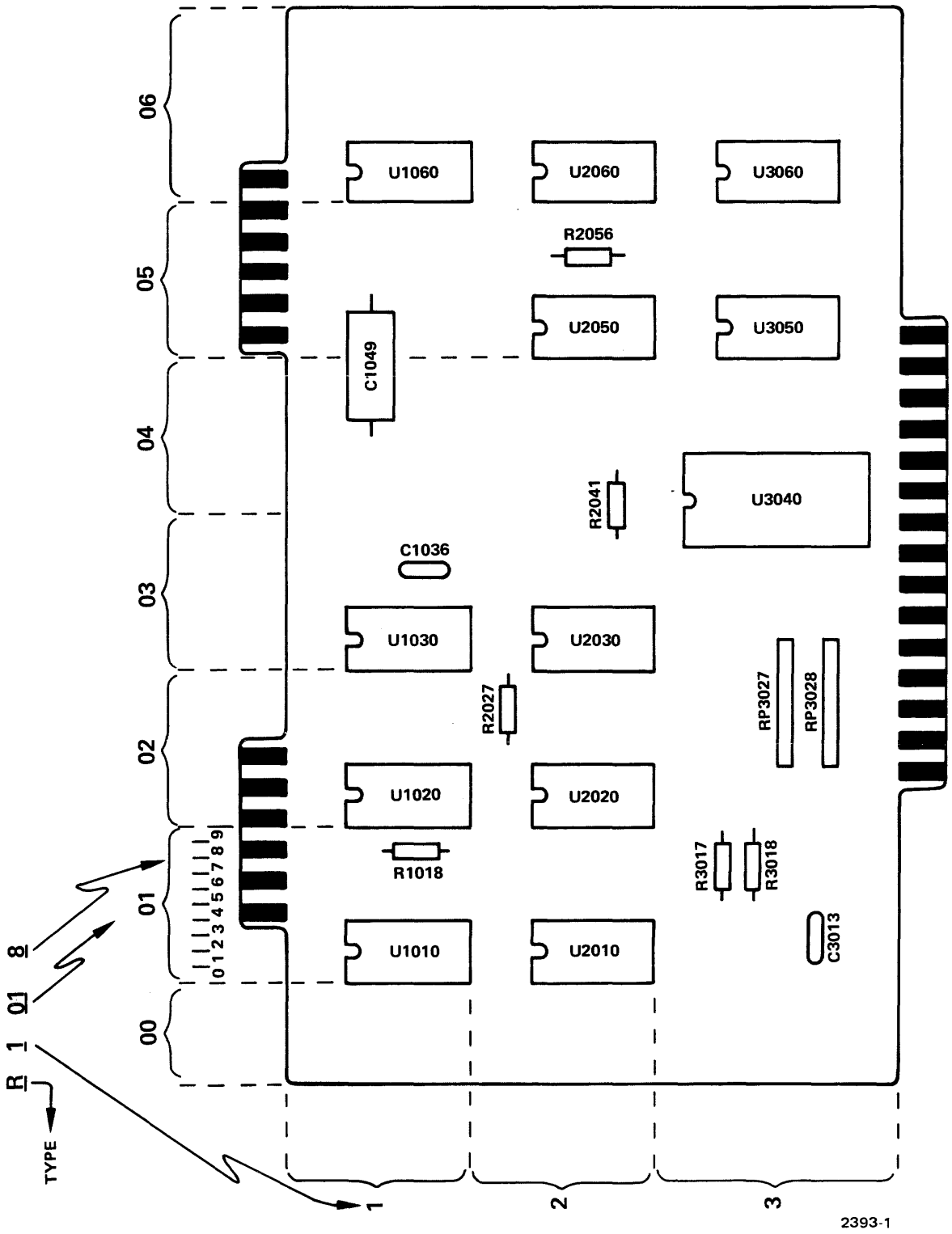


Fig. 1-3. Circuit Number Guide.

Section 2

RS-232-C PORTS

GENERAL

The 8001/8002 μProcessor Lab has four RS-232-C I/O ports. These ports are used for transferring data between the μProcessor Lab and peripheral equipment. Each of these ports is associated with specific device names in the software system. Electrical specifications for these ports conform to the RS-232-C standards and can be found in the 8001/8002 μProcessor Lab Service Manual. Specific hardware and software port interface information is found in the section on the originating module.

The ports are set up for asynchronous serial data transmission. The byte structure is: one start bit, eight data bits and one stop bit. More stop bits are ignored when received. The eighth data bit, or parity bit, is not used.

The jacks for the four I/O ports are located on the rear panel of the main chassis as shown in Fig. 2-1.

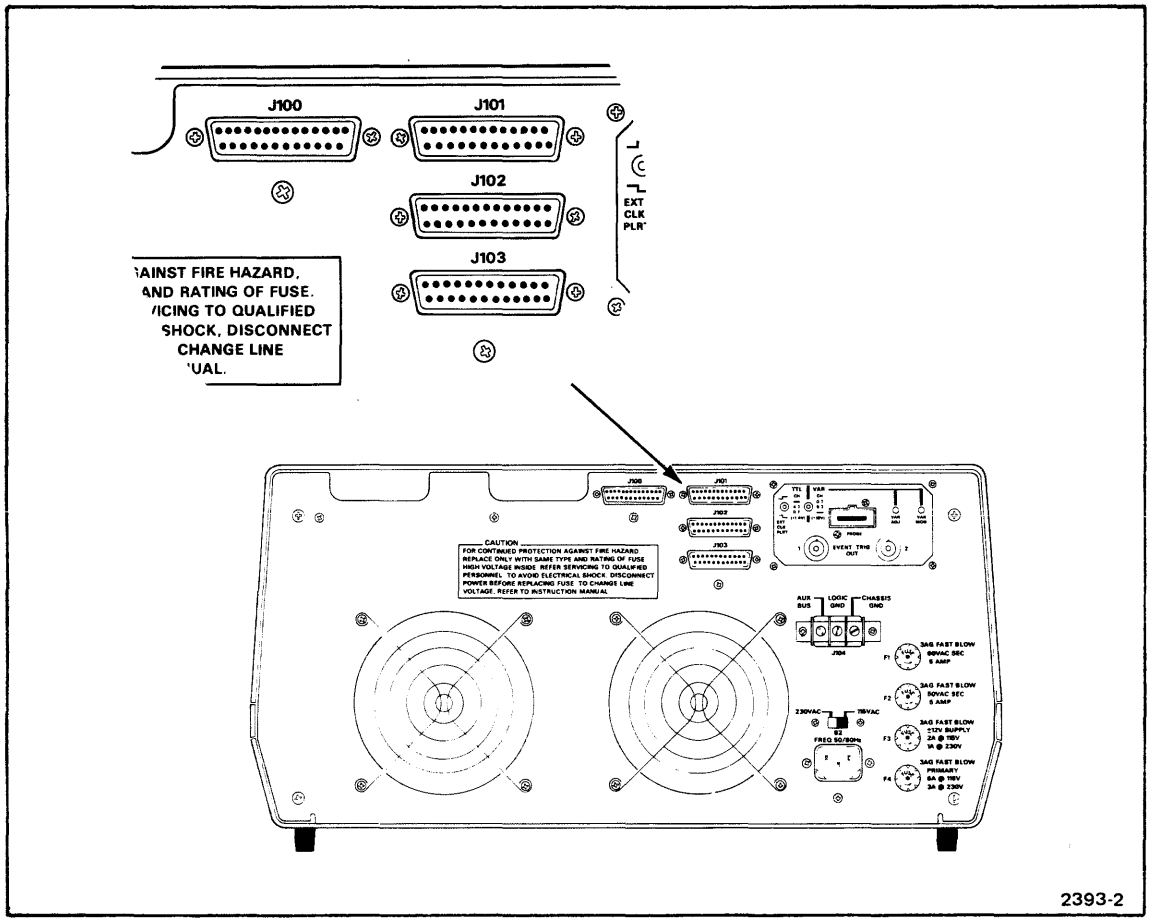


Fig. 2-1. 8001/8002 μProcessor Lab RS-232-C I/O Ports.

PORT ASSIGNMENTS

Each I/O port has a specific software device assignment. Each I/O port also connects to a peripheral device by a specific jack on the rear panel of the μProcessor Lab. You can say that each jack is assigned to a specific software device.

The system console connects to jack J100. Any terminal-like device may be used as the system console if it has a keyboard, a display and an RS-232-C communications port. Two Tektronix terminals are available as options: the CT 8100 CRT Terminal and the CT 8101 Printing Terminal. The console terminal port originates from the System Processor module.

Jack J101 is usually connected to a communications modem. This allows the μProcessor Lab to serve as a remote terminal communicating with another computer system.

Jack J102 is used to connect a line printer to the μProcessor Lab. The software does not accept any input from J102. This jack provides output service only to a line printer type device. The TEKTRONIX Line Printer LP8200 is available as an option.

Jack J103 is the paper tape reader/punch connection. The Remex RAR 8050 is recommended for use with the system.

Communications, Line Printer, and Paper Tape Reader/Punch ports originate from the System Communications module.

The software device names are an indication of the intended use for each jack. The software device names and their jack assignments are shown in Table 2-1.

Table 2-1
Jack and Device Assignment

Jack Number	Input Device	Output Device	Device Description
J100*	CONI	CONO	Console Terminal
J101	REMI	REMO	Communications Module
J102	---	LPT1	Line Printer
J103	PPTR	PPTP	Paper Tape Reader/Punch

*Device TTYR (Teletypwriter reader) may also be used for input to J100.

Section 3

SYSTEM PROCESSOR MODULE

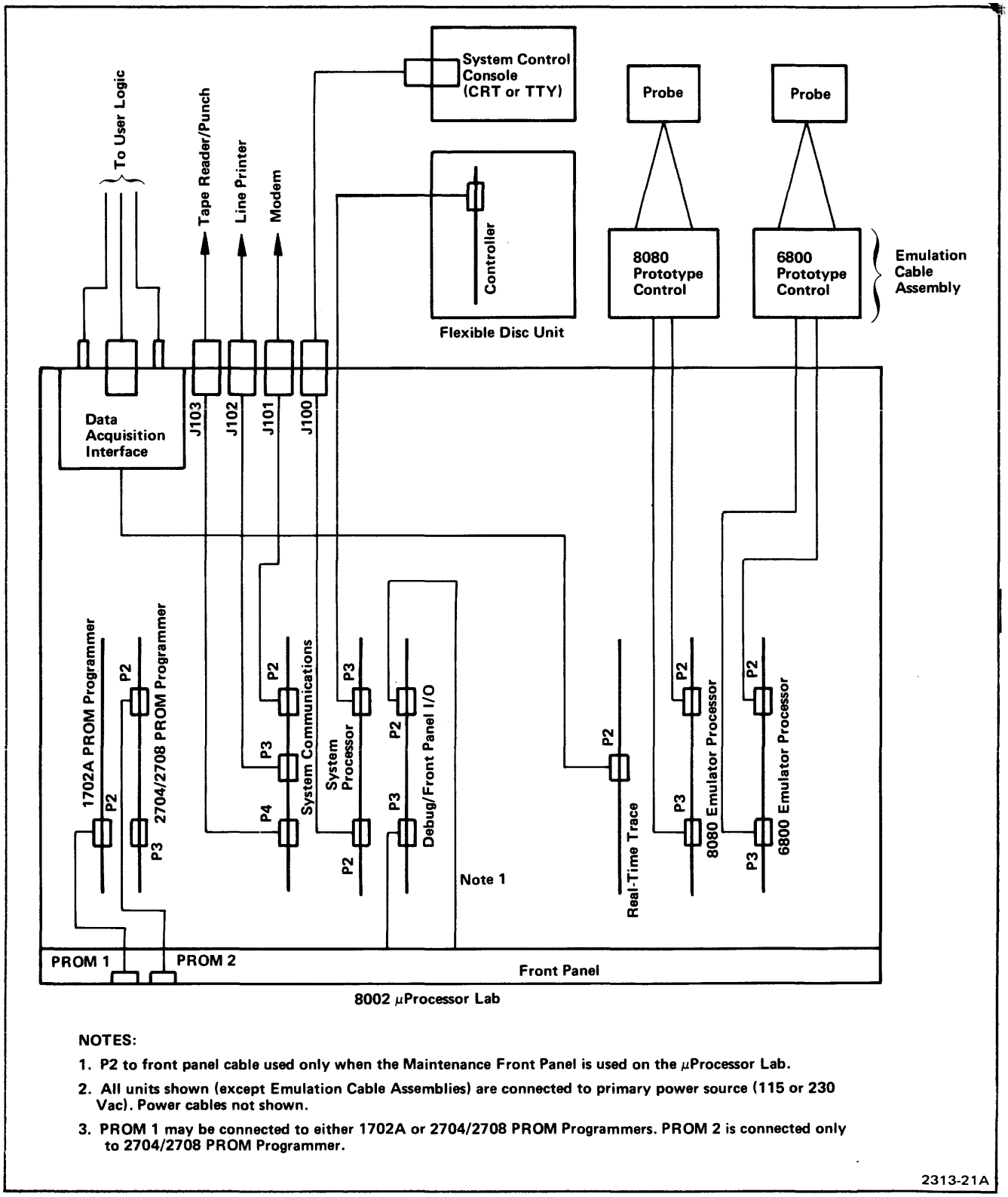
INSTALLATION

The System Processor module plugs into any System section of the motherboard. For cabling convenience, it is normally plugged into J8. The module connector is offset, ensuring that the module cannot be plugged in backwards. All power requirements are supplied through the motherboard. A standard flat ribbon 26 pin I/O cable attaches to the top edge connector P2 for terminal input/output. A ribbon cable from the Flexible Disc Unit attaches to the top edge connector P3 (see Fig. 3-1 for an interconnect diagram). Care should be taken that pin 1 of the cable (red stripe) aligns with pin 1 of the edge connector. Pin 1 is to the left as viewed from the component side of the board.

DESCRIPTION

General

The terminal I/O port (J100) is interfaced with a UART and is located on the rear panel of the main chassis as shown in Fig. 3-2. This port is configured to be RS-232-C interface type D with Data Terminal Ready (DTR) sensed. See Table 3-1. All of the referenced RS-232-C control signals are used in the μProcessor Lab, and any equipment interfaced to the lab must be properly configured.



NOTES:

1. P2 to front panel cable used only when the Maintenance Front Panel is used on the μProcessor Lab.
2. All units shown (except Emulation Cable Assemblies) are connected to primary power source (115 or 230 Vac). Power cables not shown.
3. PROM 1 may be connected to either 1702A or 2704/2708 PROM Programmers. PROM 2 is connected only to 2704/2708 PROM Programmer.

Fig. 3-1. 8001/8002 μProcessor Lab System Interconnect Diagram.

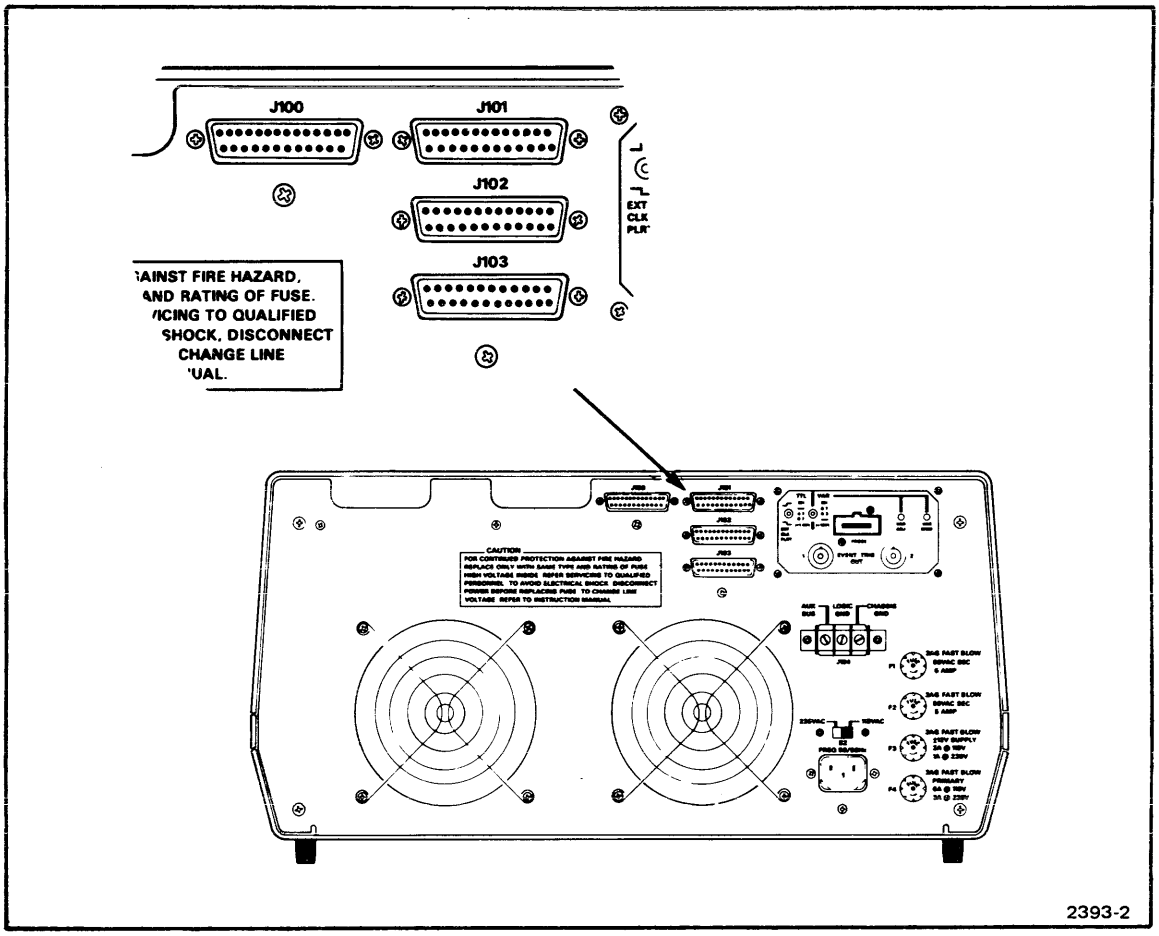


Fig. 3-2. 8001/8002 μProcessor Lab RS-232-C I/O Ports.

When large blocks of data are transferred to a device with limited buffer space, the RS-232-C control signals must be used to cause a data transmission delay. The delay allows the buffer to be emptied.

Table 3-1
RS-232 Control Signals

Mnemonic	Signal Name	Use	Ckt.	Pin No. Assignments
GND	Protective Ground	Chassis	AA	1
TDATA	Transmitted Data	Data flow from terminal to modem	BA	2
RDATA	Received Data	Data flow from modem to terminal	BB	3
RTS	Request To Send	Control signal from terminal asking for permission to send data	CA	4
CTS	Clear To Send	Control signal sent to terminal indicating transmission can begin	CB	5
DSR	Data Set Ready	Control signal sent to terminal indicating data equipment is operational	CC	6
SGND	Signal Ground	Ground line for all signals	AB	7

Software Transformation in TEKDOS When Using ASCII Transfers

Some special control characters are transformed within the μProcessor Lab when either entering or exiting the individual RS-232-C ports. The transformations may be different for input and output, and for different ports. These transformations are used to accomodate the particular device envisioned to reside at the port.

Before attaching a device to any of these ports, these transformations have to be considered, and any changes necessary to accomodate a special device must be accomplished within the external device.

Control Character Abbreviations For The Following Description:

CR	Carriage Return
LF	Line Feed
XON	Transmitter ON
XOF	Transmitter OFF
NUL	Null Character
BRK	Break Character
EOL	End of Line
EOF	End of File
DEL	Delete Character
BS	Backspace Character
ESC	Escape Character
CTRL–Z	Control Z Character
KL	Kills Current Line

Console Port (J100)

Software Device Names:

TTYR – input (teletype reader or equivalent)
CONI – input (keyboard terminal)
CONO – output (keyboard terminal)

Function of Port:

Console I/O port equipped to handle either EIA or TTY interfaced terminals.

Table 3-2
Port J100 EIA, TTY Pin Assignment

	Pin Assignments	Function
(EIA Pins)	2 EIA REC DATA	INPUT
	3 EIA XMIT DATA	OUTPUT
	4 CA *	REQUEST TO SEND (+5.2 V 2.2k)
	5 CB *	CLEAR TO SEND (+5.2 V 2.2k)
	6 CC *	DATA SET READY (+5.2 V 2.2k)
	7 EIA – GND	EIA GROUND
	20 CD *	DATA TERMINAL READY (+5.2 V 2.2k)
(TTY Current Loop Pins)	16 TTRDR –	TAPE READER CONTROL OUT
	18 TTRCV –	TTY CURRENT LOOP OUTPUT
	14 TTX –	TTY CURRENT LOOP INPUT
	13 TTX+ *	620 OHM TO +12 V
	15 TTRDR+ *	47 OHM TO +12 V
	17 TTRCV+ *	620 OHM TO +12 V

*Indicates pulled up to power supply only.

Note: This port is not a true RS-232-C port, but is designed to be the main system console port equipped to handle TTY current loop or EIA RS-232-C keyboard terminals.

Software Transformations:

Table 3-3
Port J100 Software Transformations

	Character	Transformations	Status Effect
In to J100	CR	CR, LF, XOF, NUL, NUL, NUL	EOL
	ESC	CR, LF, XOF, NUL, NUL, NUL	BRK, EOL
	CTRL–Z	CR	EOL, EOF
	BS	echo BS & delete char	
	DEL	echo & delete last char	
	XOF	echo XON	
	LF, NUL	ignored	
Out from J100	CR	CR, LF, XOF, NUL, NUL, NUL	

TTYR Treats all control characters in the same manner as CONI. In addition, an ASCII read from TTYR: 1) enables the TTY reader bit in the I/O port that starts the reader on a minicomputer-modified ASR-33, and 2) sends XON to CONO.

To Change the Console Output Port Characteristics:

These software changes apply to "TEKDOS Version 2.1." Check memory location to ensure proper data value before making changes.

A. Removal of XOF character (DC3)

In this port the carriage return is normally followed by an XOF character for operation with the TEKTRONIX 4923 Digital Cartridge Tape Recorder or similar device. To remove this:

Change location 2DF2 from a value of 13 to 00.

B. Select the number of fill characters. The default value is 4 fill characters.

Table 3-4
Port J100 Output Characteristics

Location	Default 4 Fills	Number of Fill Characters			
		3	2	1	0
2D46	05	04	03	02	01
2DB2	06	05	04	03	02

Baud Rate Selection

A thumbwheel switch is provided on the system processor board to select the baud rate. See Table 3-5. Data format is selectable for binary or ASCII format at 110 baud. The removal of jumper J1 provides binary format for all bauds. See Fig. 3-3 for jumper J1 and baud select thumbwheel switch locations.

Table 3-5
Port J100 Baud Select

Switch Position	Selected Baud Rate	Data Format
0, 1, 2	not used	
3	2400	Start 0123456 Parity Stop
4	1200	Start 0123456 Parity Stop
5	600	Start 0123456 Parity Stop
6	300	Start 0123456 Parity Stop
7	150	Start 0123456 Parity Stop
8	110	Start 0123456 Parity Stop Stop
9	110	Start 0123456 Parity Stop Stop

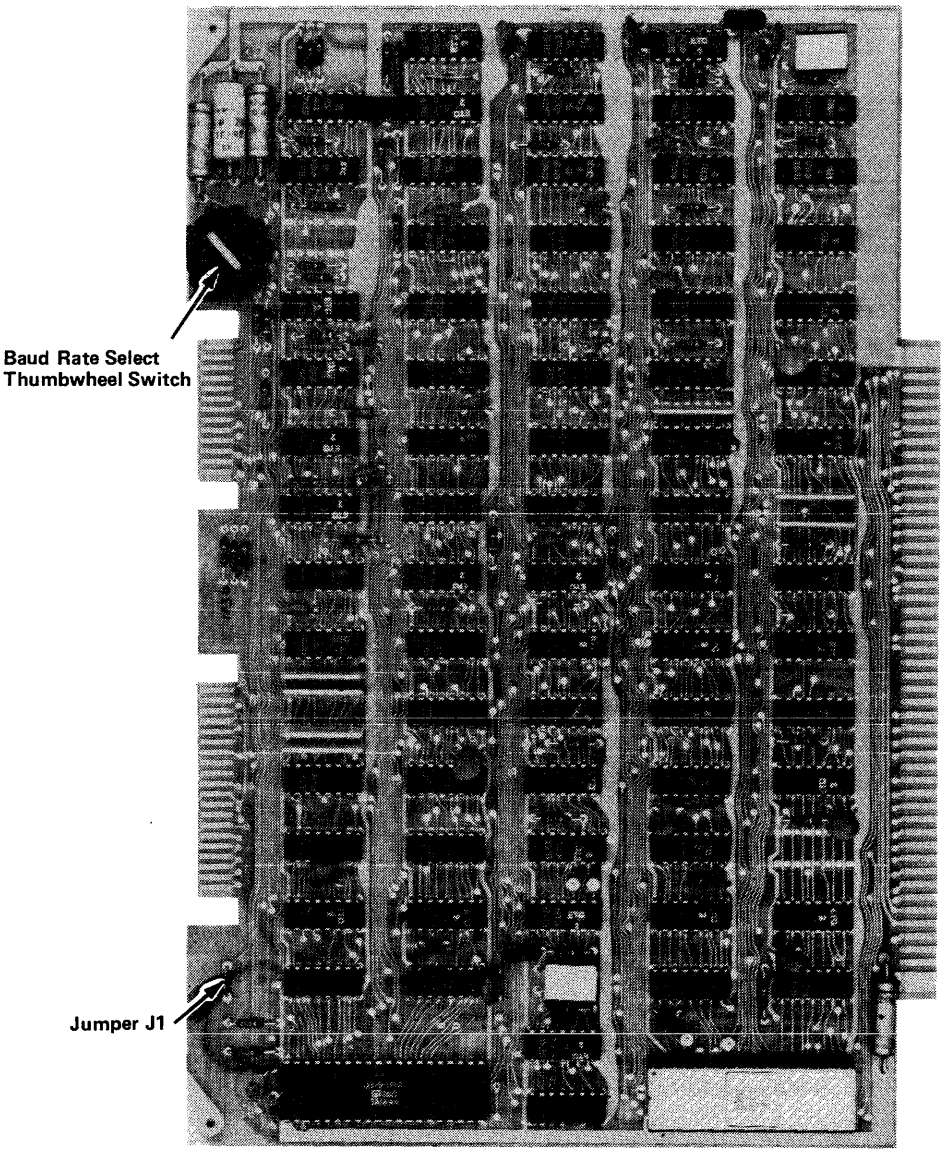


Fig. 3-3. 8001/8002 System Processor Module. 2393-3

Section 4

8001 SYSTEM MEMORY MODULE

INSTALLATION

The 8001 System Memory module may be inserted into any available slot in the system section of the μProcessor Lab motherboard. The card connector is offset, ensuring that it cannot be inserted backwards. All power requirements are supplied through the motherboard. Fig. 4-1 illustrates the physical layout.

DESCRIPTION

The 8001 System Memory module contains the main operating software (TEKOPS) for the μProcessor Lab. This System Memory consists of 6k bytes of ROM for the main operating system, 2k bytes of RAM, and 16 2k byte selectable banks of ROM. An additional 1k byte of PROM is available to allow patching of the 6k byte main operating system or the bank-switched ROM. Patches are made to update as many as 96 firmware changes of 2, 4, or 8 bytes. More ROM may be gained by installing up to three more memory modules containing only the 16 selectable 2k byte banks of ROM.

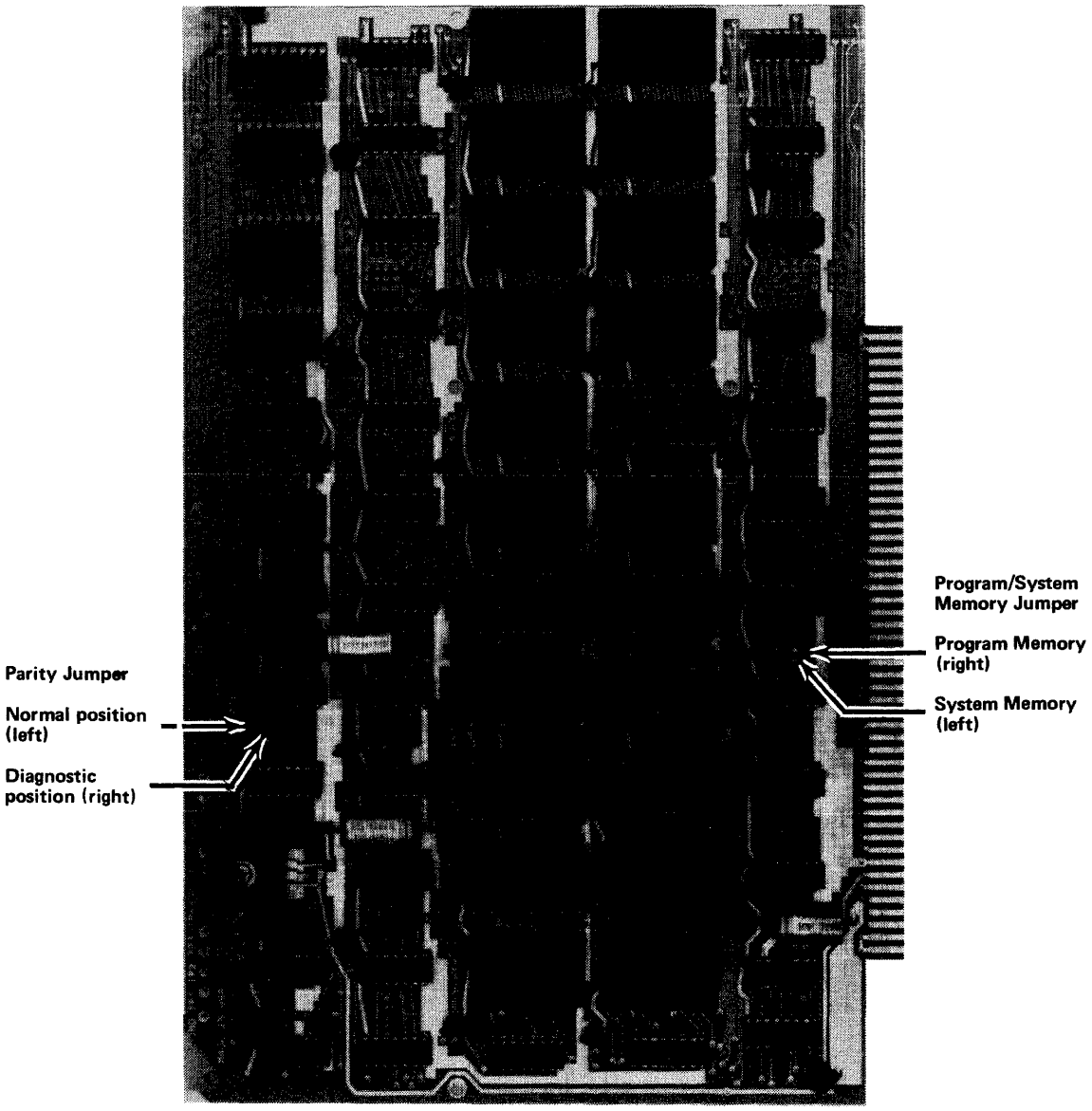


Fig. 4-1. 8001 System Memory Module.

JUMPERS

The 8001 System Memory module was designed to accept a variety of memory microcircuits.

Table 4-1 describes the jumper changes required to configure the memory module for different sets of microcircuits. For example, to utilize the 9316B 2k x 8 bit ROM, the chart shows that a 2.2k resistor must be loaded onto the module; the –5 volt regulator is not loaded; the 3 watt resistor is not loaded; jumper U→V is not connected; and jumpers are connected between I→K, W→Y, S→R, P→Q, L→M, and AA→AC.

Table 4-1
8001 System Memory ROM Configuration

	2.2k	–5 volt regulator	3W resistor note 1	U→V note 5	I note 4	W note 3	S	P	L	AA
Production 65317	NL	L	NL	NL	K	X	T	O	M	AB
Production 9316B	L	NL	NL	NL	K	Y	R	Q	M	AC
Prototype 2708	NL	L	L	NL		Y	T		N	AB
Low 8 banks*					M			Q		
High 8 banks*					J			Q		
Prototype 2708 (Bank Switch)			L	NL	M/J		T	Q	N	
65317						X				AB
8613						Y				AC
Prototype 2716				NL	K		R	Q	M	AC
Prototype 2716 (Bank Switch)			NL	NL	K		R	Q	M	
65317						X				AB
9613						Y				AC
6831B	L	L	NL	NL	K	Y	R	Q	M	AC

*Each memory module consists of 8 banks of 2k bytes per bank of selected ROM.

Notes:

1. Cut run and add resistor selected to give a 2-1/2 volt drop around the −5 volt regulator.
2. NL = Not Loaded
   L = Loaded
3. When W→X don't load cap C410.
4. I→M low 8 banks/I→J high 8 banks. (2708 only)
5. For future use with a faster 2650.

Section 5

PROGRAM MEMORY/8002 SYSTEM MEMORY MODULE

INSTALLATION

The 16k RAM Program Memory module may be plugged into any available slot in either the System or Program section of the μProcessor Lab motherboard. The card connector is offset, ensuring that it cannot be inserted backwards. All power requirements are supplied through the motherboard. Fig. 5-1 illustrates the physical outline.

SWITCH AND JUMPER OPTIONS

Reference Fig. 5-1 for switch and jumper locations.

A DIP bank of 4 two-position slide switches (S4163) allows setting of four options. These options are module base address (A14, A15), high or low byte of word memory, and system or program memory. See Table 5-1. The System/Program Memory switch automatically enables the PROM operation when in the System Memory position.

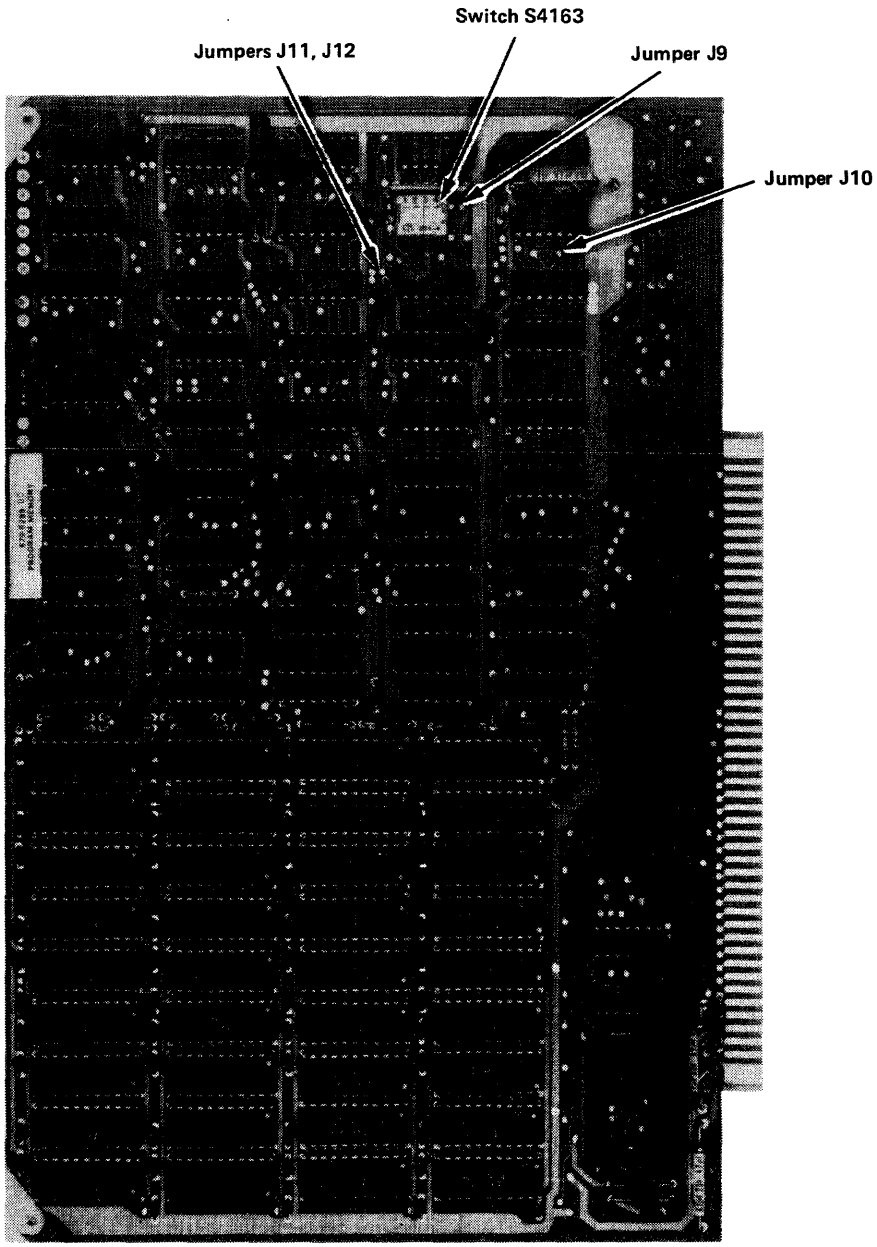


Fig. 5-1. Program Memory/8002 System Memory Module.

Table 5-1
Program Memory/8002 System Memory Switch Options

Switch	Description	Switch on Indicates
S4163-1	A14 (16k Weight)	A14 = 1
S4163-2	A15 (32k Weight)	A15 = 1
S4163-3	System/Program	Program Memory
S4163-4	High/Low Byte	High Byte

Table 5-1A
Memory Module Option Switch Functions

S4163-1 S4140-2	S4163-2 S4140-1	Memory Module Starting Address
Off	Off	0000
On	Off	4000
Off	On	8000
On	On	C000

Note: Switch S4163 settings apply to the Program Memory 1 8002 System Memory Module. Switch S4140 settings apply to the High Speed Memory module.

If the 16k RAM memory board is to be used as system memory then jumper J11 must be installed and jumper J12 must be deleted. See Table 5-2.

Table 5-2
Program Memory/8002 System Memory Mode Jumpers

Jumper	System Memory	Program Memory
J11	installed	deleted
J12	deleted	installed

Word Mode

The 16k RAM memory is an 8-bit byte memory. For use as word memory with 16-bit emulator processors, two memory modules with the same module address must be used. One module must be selected as the high byte and the other module as the low byte (switch S4163-4). The word mode option is set by installing jumper J9 and deleting jumper J10. See Table 5-3.

Byte oriented processors are still able to access both memories by reading each one alternately.

Table 5-3
Program Memory Byte/Word Mode Jumpers

Jumper	Byte Memory	Word Memory
J9	deleted	installed
J10	installed	deleted

9900 WORD MODE HARDWARE MODIFICATION

This hardware modification is only to be performed on memory boards converted to word mode for use with the 9900 emulator processor. Once the boards have been modified, byte oriented processors can continue to be used provided both boards are used together. In this case the modified boards will be accessed by reading each one alternately.

Modification Procedure:

1. Cut runs to pins 1 and 2 of U5150
2. Cut run to pin 12 of U4170
3. Cut jumper J10 (located between U5150 and U5160)
4. Connect jumper between pins 2 and 4 of U5150
5. Connect jumper between pin 1 of U5150 and pin P1-80
6. Connect jumper between pin 3 of U5150 and pin 12 of U4170
7. Connect a 560 ohm resistor (Tek P/N 315-0561-00) between pins 3 and 14 of U5150

See Fig. 5-2 for location of runs.

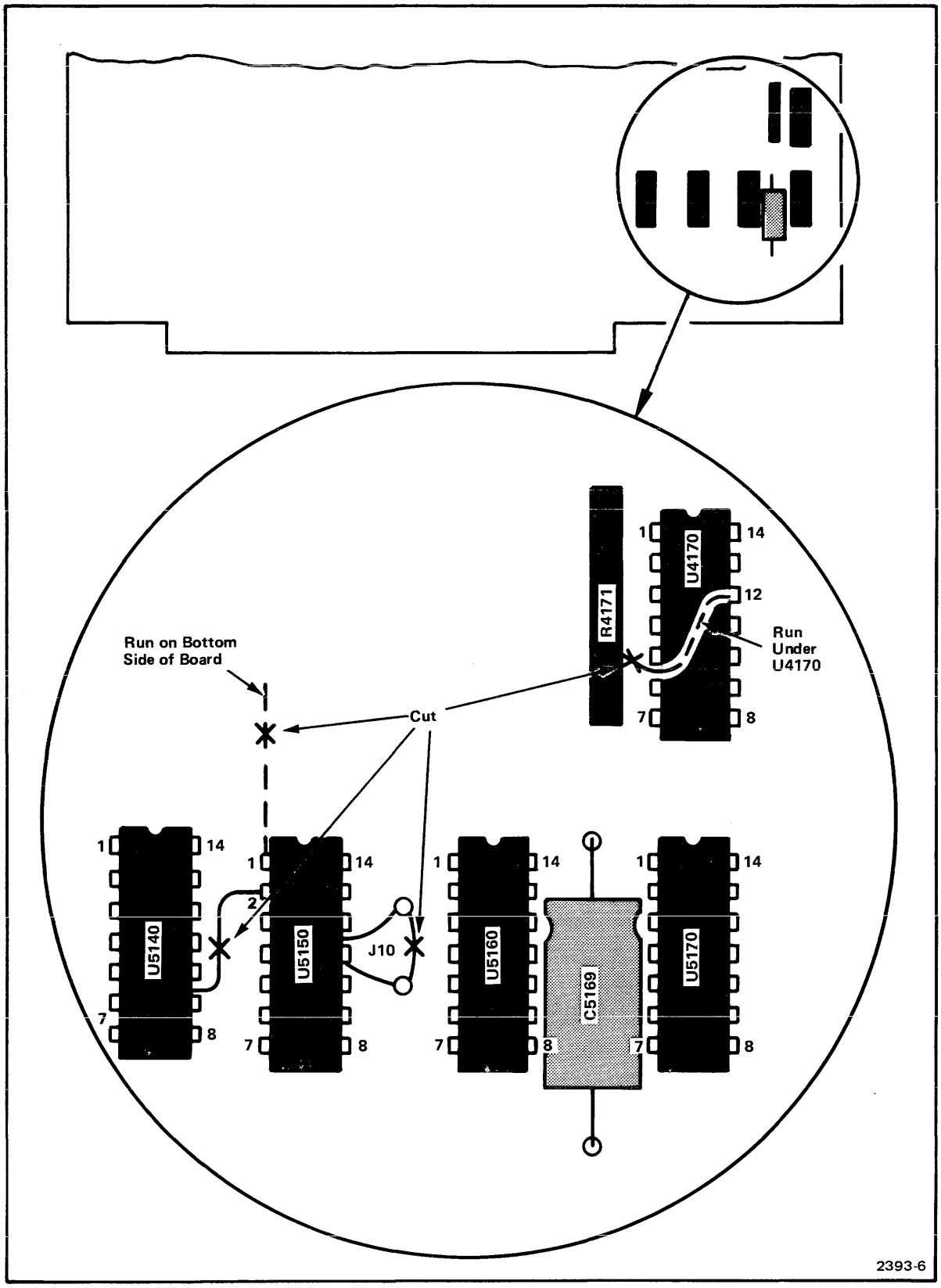


Fig. 5-2. Program Memory—9900 Word Mode Modification.

Section 6

HIGH SPEED MEMORY MODULE

INSTALLATION

The 16k High Speed Memory module may be installed in any available slot in either the system or Program section of the μProcessor Lab motherboard. The card is offset, ensuring that it cannot be inserted backwards. All power requirements are supplied through the motherboard. Fig. 6-1 illustrates the physical layout.

An 82S115 PROM programmed as per Fig. 6-2 (the TEKDOS Bootstrap loader) must be added if the High Speed Memory is to be used as system memory. The PROM should be inserted into socket U7050, and switch S4140-5 should be on.

SWITCH AND JUMPER OPTION

A DIP bank of 6 two-position slide switches (S4140) allows setting of six options. These options are module base address (A14, A15), word or byte memory, high or low byte of word memory, system or common memory, and residence of the boot PROM. See Table 6-1.

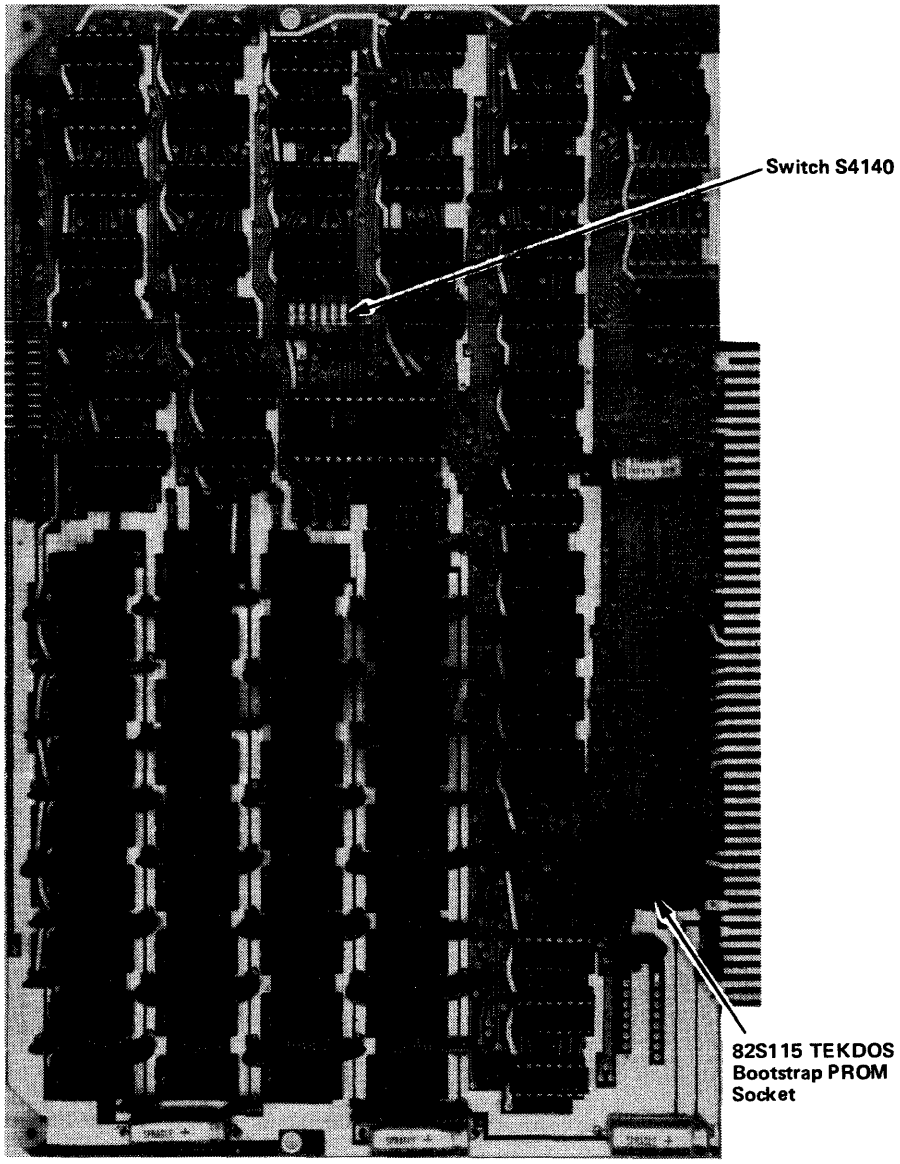


Fig. 6-1. High Speed Memory Module.

```
0000=00 01 1F 00 10 CC 10 04 59 1B 80 00 9C 4F 3B 07
0010=18 40 E4 00 10 CC 01 84 00 10 0C 6C DB 80 00 9C
0020=62 3B 05 98 7F E7 58 3B 00 F0 CF EB 54 68 3B 00
0030=06 00 10 CC 01 10 CC C3 20 17 36 44 EB 54 17 7C
0040=9A EA 54 EA D6 17 7C 1A EA 54 EA D4 07 04 88 01
0050=00 01 FF 88 00 00 01 5B 1B 05 27 63 D9 24 18 21
0060=3B 6F 5B 02 18 05 E7 19 3B 24 3B 04 06 EB D4 A9
0070=40 0F 07 1B 04 87 06 06 2A 3B 00 05 FF 75 00 07
0080=5D 10 5A 10 57 10 54 10 51 10 4E 10 4B 10 48 10
0090=45 10 42 10 3F 10 3C 10 39 10 36 10 33 10 30 10
00A0=2D 10 2A 10 27 10 24 10 21 10 1E 10 1B 10 18 10
00B0=15 10 12 10 0F 10 0C 10 09 10 06 10 03 10 80 00
00C0=BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B
00D0=BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B
00E0=BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B
00F0=BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B BE 1B
```

Fig. 6-2. TEKDOS Bootstrap Loader. 2393-8

Table 6-1
High Speed Memory Switch Options

Switch	Description	Switch on Indicates
S4140-1	A15 (32k Weight)	A15 = 1
S4140-2	A14 (16k Weight)	A14 = 1
S4140-3	16 Bit Word/8 Bit Byte Memory	Word Memory
S4140-4	System/Program	Program Memory
S4140-5	Boot PROM Resident	PROM Resident
S4140-6	High/Low Byte	High Byte

Table 6-1A
Memory Module Option Switch Functions

S4163-1 / S4140-2	S4163-2 / S4140-1	Memory Module Starting Address
Off	Off	0000
On	Off	4000
Off	On	8000
On	On	C000

Note: Switch S4163 settings apply to the Program Memory 1 8002 System Memory Module. Switch S4140 settings apply to the High Speed Memory module.

Word Mode

The High Speed memory is an 8-bit byte memory. For use as word memory with 16-bit emulator processors, two memory modules with the same module address must be used. One module must be selected as high byte and the other module as low byte (switch S4140).

Byte oriented processors are still able to access both memories by reading each one alternately.

Section 7

SYSTEM COMMUNICATIONS MODULE

INSTALLATION

The System Communications module plugs into any available System section slot of the motherboard (J3-J8). The module connector is offset, enduring that it cannot be inserted backwards. All power requirements are supplied through the motherboard. A standard flat ribbon 25 conductor cable may be attached to the top edge connectors P2 through P4 for serial RS-232-C input/output. P2 is primarily designated for modem operation. The cable provides for a rear panel 25 pin connection. Care should be taken that pin 1 of the cable (red stripe) and pin 1 of the edge connector is to the left when viewed from the component side of the module.

DESCRIPTION

The System Communications module provides for two features, Memory Mapping and RS-232 I/O Communication Ports.

MEMORY MAPPING

Memory mapping defines the users memory address space to be either the μProcessor Lab program memory, the prototype memory or any combination.

RS-232-C I/O COMMUNICATIONS PORTS

General

The System Communications module provides three RS-232-C I/O ports. Each of these I/O ports has been assigned a specific device by software and has a jack assignment on the rear panel of the 8001/8002 μProcessor Lab. See Table 7-1, Jack and Device Assignments.

Table 7-1
Jack and Device Assignments

Jack Number	Input Device	Output Device	Device Description
J101	REMI*	REMO*	Communications Module
J102	———	LPT1*	Line Printer
J103	PPTR*	PPTP*	Paper Tape Reader/Punch

*Software device name.

Jack J101 is usually connected to a communications modem. This allows the μProcessor Lab to serve as a remote terminal communicating with another computer system.

Jack J102 is used to connect the line printer to the μProcessor Lab. The TEKTRONIX Line Printer LP 8200 is available as an option.

Jack J103 is the paper tape reader/punch connection. The Remex RAR 8050 is recommended for use with the system.

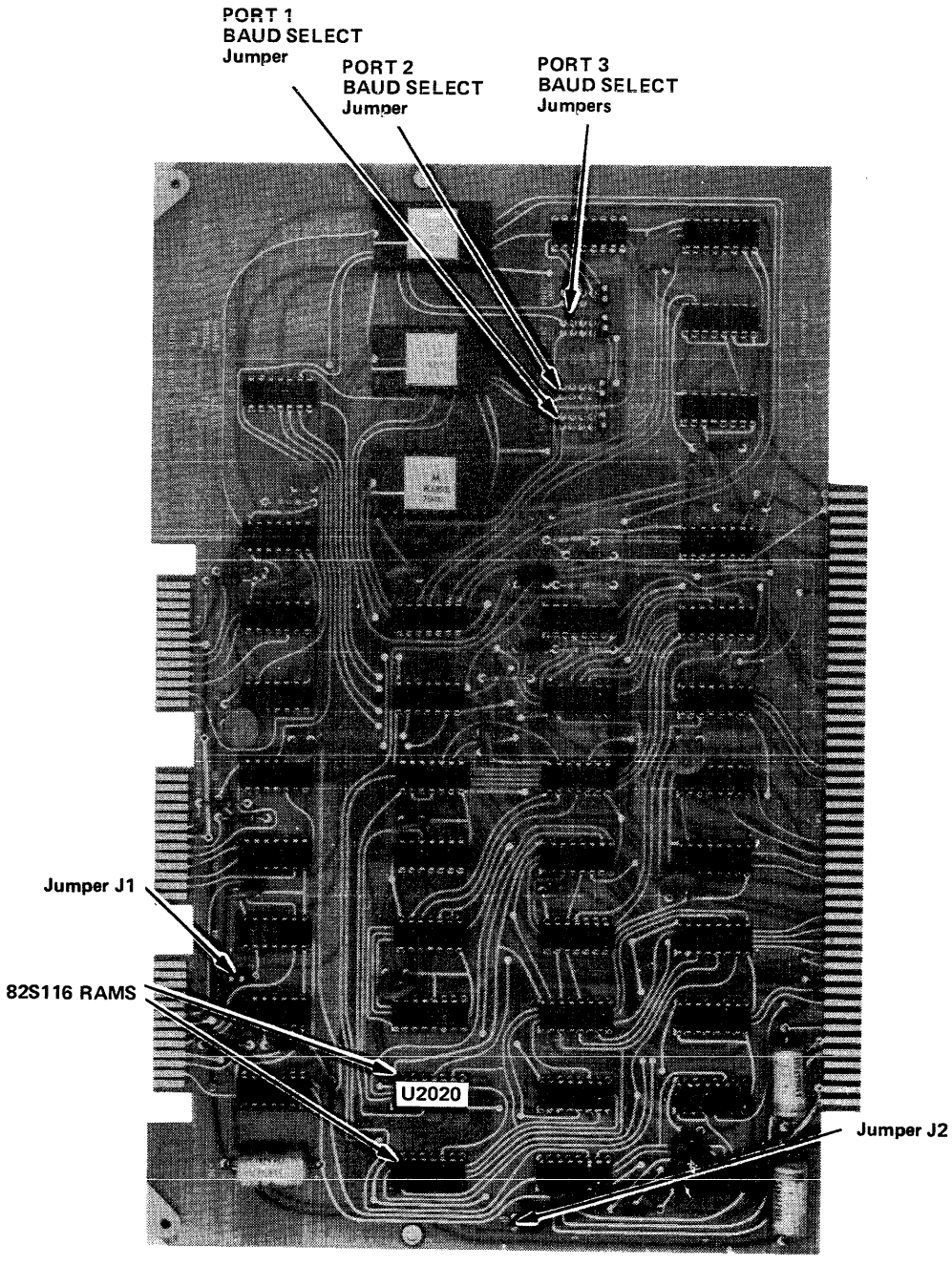


Fig. 7-1. System Communications Module.

The memory map consists of a 512 X 1 bit RAM which contains a bit map defining the user's memory address space.

Bit Map Options

The bit map defines 512 blocks of 128 bytes each in the 64k addressable space. Blocks are defined as follows: Block 0 – bytes 0 to 127, Block 1 – bytes 128 to 255, etc. The 64k address space can also be divided into 256 blocks of 256 bytes each. Block 0 – bytes 0 to 255, etc.

128 byte/block operation is selected when both RAMs (825116) are installed and J2 is in position "B".

256 byte/block operation is selected when J2 is in position "A" and U2020 is removed. See Fig. 7-1 for jumper locations.

The ports are set up for asynchronous serial data transmission. The byte structure is as follows: one start bit, eight data bits and one stop bit. More stop bits are ignored when received. The eighth data bit, or parity bit, is not used.

The jacks for the three I/O ports are located on the rear panel of the main chassis as shown in Fig. 7-2.

I/O Port Interfacing

Each I/O port is interfaced with a Motorola 6850 ACIA. These ports are configured to be RS-232-C interface type D with Data Terminal Ready (DTR) sensed. See Table 7-2.

All of the referenced RS-232-C control signals are used in the μProcessor Lab, and any equipment interfaced to the lab must be properly configured.

When large blocks of data are transferred to a device with limited buffer space, the RS-232-C control signals must be used to cause a data transmission delay. The delay allows the buffer to be emptied. These RS-232-C control signals have to be used and sensed in both hardware and software.

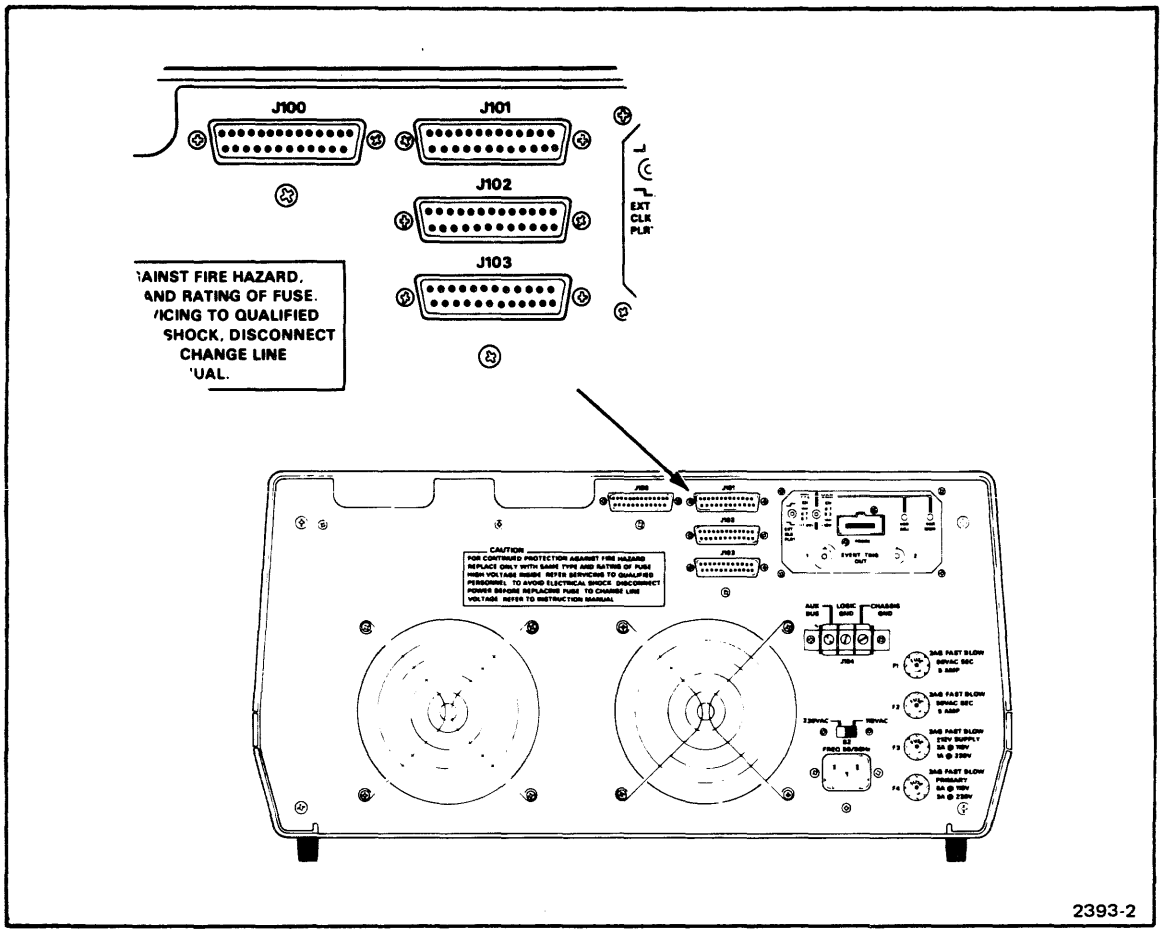


Fig. 7-2. 8001/8002 μProcessor Lab RS-232-C I/O Ports.

Table 7-2
RS-232 Control Signals

Mnemonic	Signal Name	Use	Ckt.	Pin No. Assignments
GND	Protective Ground	Chassis	AA	1
TDATA	Transmitted Data	Data flow from terminal to modem	BA	2
RDATA	Received Data	Data flow from modem to terminal	BB	3
RTS	Request To Send	Control signal from terminal asking for permission to send data	CA	4
CTS	Clear To Send	Control signal sent to terminal indicating transmission can begin	CB	5
DSR	Data Set Ready	Control signal sent to terminal indicating data equipment is operational	CC	6
GND	Signal Ground	Ground line for all signals	AB	7

Software Transformation In TEKDOS When Using ASCII Transfers

Some special control characters are transformed within the μProcessor Lab when either entering or exiting the individual RS-232-C ports. The transformations may be different for input and output, and for different ports. These transformations are used to accomodate the particular device envisioned to reside at the port.

Before attaching a device to any of these ports, these transformations have to be considered, and any changes necessary to accomodate a special device must be accomplished within the external device.

Control Character Abbreviations For The Following Description:

CR	Carriage Return
LF	Line Feed
XON	Transmitter ON
XOF	Transmitter OFF
NUL	Null Character
BRK	Break Character
EOL	End of Line
EOF	End of File
DEL	Delete Character
BS	Backspace Character
ESC	Escape Character
CTRL-Z	Control Z Character
KL	Kills Current Line

MODEM PORT (J101)

Software Device Names: REMI – input (Remote input)
REMO – output (Remote output)
COMM – command

Function of Port: Makes μProcessor Lab look like a terminal. All other ports make the μProcessor Lab look like a controller. Therefore, this port requires a modem or a null modem to attach other equipment.

Control Outputs: The following RS-232-C control signals are provided:

CA	REQUEST TO SEND	Pin No. 4	fully implemented
CD	DATA TERM READY	Pin No. 20	tied to +12 V

Control Inputs: The following RS-232-C control signals are sensed:

CF	REC. LINE SIG. DET.	Pin No. 8	
CB	CLEAR TO SEND	Pin No. 5	J-1 in position 'A'
CC	DATA SET READY	Pin No. 6	J-1 in position 'B'

(J-1 is a selectable jumper for either CB or CC)

Software Transformations:

Table 7-3
Port J101 Software Transformations

	Character	Transformations	Status Effect
Out From J101:		none	
In To J101:	CR	CR	EOL
	CTRL–Z	CTRL–Z	KL, EOF
	DEL, LF, NUL	ignored	

Note: This port makes the μProcessor Lab appear like a terminal. All control of data transfers has to be on the controller end via software. The COMM command uses SVC calls to accept the formatted data and put it in memory through this port. This is the port that is recommended to be used with computer transfers (either time – share using a modem or direct using a null modem).

Null Modem. A Null Modem can be constructed from two RS-232-C 25 pin female connectors. Wire the two connectors according to Fig. 7-3.

Line Printer Port (J102) and Paper Tape Port (J103)

Software Device Names:	Port (J102)	Port (J103)
	LPT1 – out	PPTR – in
		PPTP – out

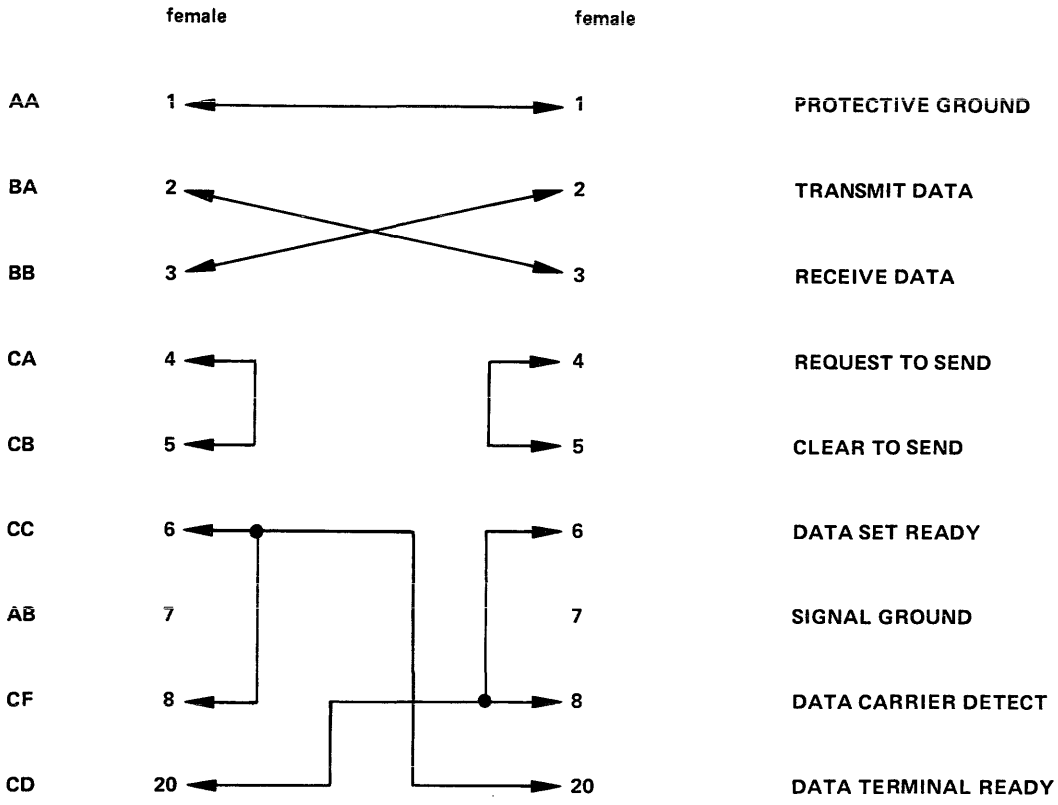


Fig. 7-3. Null Modem. 2392-10

Function of Ports: These ports require a terminal type device to be attached. The μProcessor Lab appears like a controller to anything hooked up to them.

J102 is designed to be used with a line printer.

J103 is designed to be used with a paper tape reader/punch.

Both ports are identically configured, with only the software differing. J102 has output capability only, while J103 has both input and output capability.

Control Outputs: The following RS-232-C control signals are provided:

CB	CLEAR TO SEND	Pin No. 5
CC	DATA SET READY	Pin No. 6 tied to +12 V
CF	REC. LINE SEG. DET.	Pin No. 8 tied to +12 V

Control Inputs: The following RS-232-C control signals are sensed:

CA	REQUEST TO SEND	Pin No. 4
CD	DATA TERMINAL READY	Pin No. 20

Software Transformations:

Table 7-4

Port J102, J103 Software Transformations

	Character	Software Transformations	Status Effect
Out From J102:	CR	LF	
In To J102:		not used	
Out From J103:	CR	CR, LF	
In To J103:	CR	CR	EOL
	CTRL–Z	CTRL–Z	KL, EOF
	DEL, LF, NUL	ignored	

The communications ports (J101, J102, J103) output characters may be changed as follows:

Table 7-5
Port J101, J102, J103 Output Characteristics

Port	Device Name	Location	Default Value	CR Only	LF Only	CR,	No Fill Characters
J101	REMO	3FDC	00	00	40	80	Add the number of desired fill characters between Ø and IF to either 00, 40, or 80
J102	LPT1	3FD8	40	00	40	80	
J103	PPTP	3FDA	80	00	40	80	

These software changes apply to "TEKDOS version 2.1".

Example: Configure J102 to have both carriage return and line feed followed by 16 fill characters output whenever an end of line occurs.

Change the value of location 3FD8 to 90. 90 is the combination of 80H and 10H (16 decimal) and stands for CR, LF plus 16 fill characters.

Baud

The following baud are available on all ports:

110, 300, 600, 1200, 2400

Port J103 has independently selectable receive and transmit rates.

Jumpers

Baud selection is made possible by the use of jumpers located on the System Communications Module. Jumper functions are listed in Table 7-6.

Table 7-6
Port J101, J102, J103 Baud Selection

Port	Baud				
Port J101	110	300	600	1200	2400
Port J102	110	300	600	1200	2400
Port J103 Recv	110	300	600	1200	2400
Port J103 Xmit	110	300	600	1200	2400

A jumper is also available to control transmission of data from the ACIA of port J101. The port, jumper designation, and control offered in the A and B position are:

Port	Jumper	A	B
J101	J1	Clear To Send	Data Set Ready

See Fig. 7-1 for jumper locations.

Section 8

REAL-TIME PROTOTYPE ANALYZER

DESCRIPTION

General

The Real-Time Prototype Analyzer is an 8001/8002 μProcessor Lab option that allows users to monitor hardware and software functions during real-time execution. The Real-Time Prototype Analyzer consists of the following three sub-assemblies:

1) The Real-Time Trace module
2) The Data Acquisition Interface board
3) The Data Acquisition Probe

The Real-Time Trace module is a circuit board that plugs into the 8001/8002 μProcessor Lab motherboard. The Real-Time Trace module contains all the circuitry required to store up to 128 bus transactions. The Real-Time Trace module also issues trigger pulses and/or breakpoints upon programmed event comparisons.

The Data Acquisition Interface is a circuit board that attaches to the rear panel of the 8001/8002 μProcessor Lab. The Data Acquisition Interface contains all the buffers, drivers, and receivers that interface the Real-Time Trace module to the nine channel Data Acquisition Interface.

The Data Acquisition Probe is an active nine channel data probe. Eight of the channels are used to input data to the Real-Time Trace module. The ninth channel carries a clock signal from a prototype device. Since a data booklet is packages with the Data Acquisition Probe, no attempt will be made in this manual to describe the Probe in detail.

See Fig. 8-1 Real-Time Prototype Analyzer.

2393-18

Fig. 8-1. Real-Time Prototype Analyzer.

Data Acquisition Probe

The Data Acquisition Probe is an active nine channel logic information gathering device. The Data Acquisition Probe circuitry consists of two hybrid circuits that comprise nine low-gain FET amplifiers with differential ECL outputs. The nine Probe input channels have a characteristic input impedance of 1 megohm.

Variable input threshold voltages allow the Data Acquisition Probe to be used with ECL, TTL, or MOS circuitry. The threshold voltages used are supplied by the Data Acqusition Interface of the Real-Time Prototype Analyzer. The nine signal leads and one ground lead connect to the Probe head. One signal lead is dedicated to clock information with the remaining eight leads used for data gathering.

More complete information on the Data Acquisition Probe may be found in the data sheet received with the Probe.

Data Acquisition Interface

The Data Acquisition Interface is the interface element between the active Data Acquisition Probe and the Real-Time Trace module. Data from the Probe's eight information channels is buffered and latched by the Probe to the Data Acquisition Interface. The Data Acquisition Interface translates the information from an ECL level to a TTL level. The information is then sent through a 26-connector ribbon cable to the Real-Time Trace module.

Another function of the Data Acquisition Interface is to provide an output for the dual event comparators located on the Real-Time Trace module. The Trigger 1 and Trigger 2 signals from the Real-Time Trace module are brought to the Interface by the ribbon cable. At this point, Trigger 1 and Trigger 2 are inverted and presented to two BNC connectors at a characteristic impedance of 50 ohms.

The Data Acquisition Probe attaches to the Data Acquisition Interface at a connector on the rear panel of the μProcessor Lab (see Fig. 8-3). The Interface panel mounts flush with the μProcessor Lab rear panel. This allows access to all the controls and input/output connectors.

INSTALLATION

The Data Acquisition Interface attaches to the rear panel of the 8001/8002 μProcessor Lab. The circuit board resides inside the μProcessor Lab with the panel of the Data Acquisition Interface flush with the rear panel of the Lab as shown in Fig. 8-2. The Data Acquisition Interface should be attached to the 8001/8002 μProcessor Lab in the following manner:

1) Make sure that the main power to the μProcessor Lab is OFF.

2) Remove the three Phillips head screws along each side of the top cover of the μProcessor Lab.

3) Lift straight up on the cover of the μProcessor Lab and set it aside.

4) While facing the rear panel of the μProcessor Lab, notice the four screws holding a blank plate to the rear panel in the upper right hand corner. Remove the screws and the plate and set them aside.

5) Place the Data Acquisition Interface circuit board inside the μProcessor Lab chassis with the component side up and the panel facing the rear of the Lab.

6) Align the four screw holes in the Data Acquisition Interface panel with the four screw holes in the μProcessor Lab rear panel.

7) Thread the four screws back into the rear panel of the μProcessor Lab and tighten.

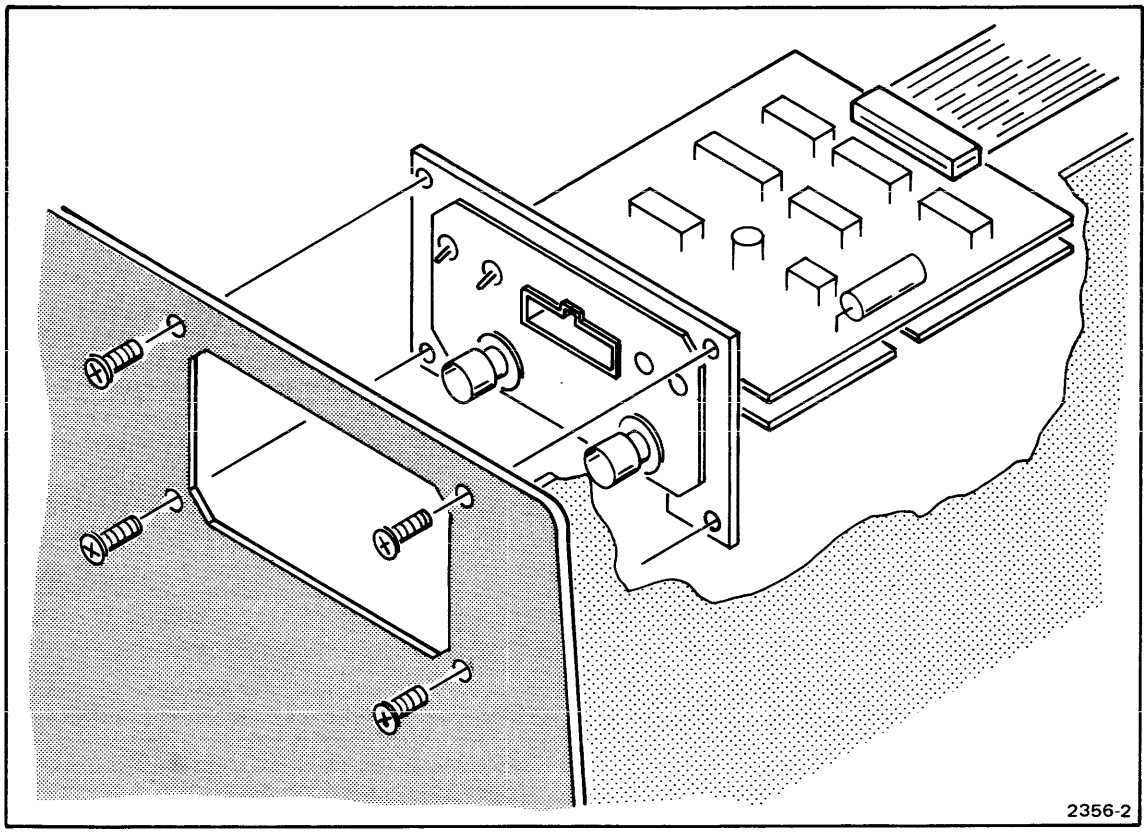


Fig. 8-2. Data Acquisition Interface Installation.

Now the Real-Time Trace module may be installed as follows:

1) While facing the front of the 8001/8002 μProcessor Lab, grasp the module by the upper edges with the component side facing left.

2) Slide the module down the guide channels labeled J15 (for cabling convenience).

3) As soon as P1 (the lower edge connector) of the Real-Time Trace module reaches the motherboard connector, press down firmly and evenly on the top edge of the module until the module snaps into place.

4) Attach the ribbon cable from the Data Acquisition Interface to the Real-Time Trace module edge connector P2. Insure that pin 1 of the ribbon cable (red stripe) and pin 1 of the edge connector align.

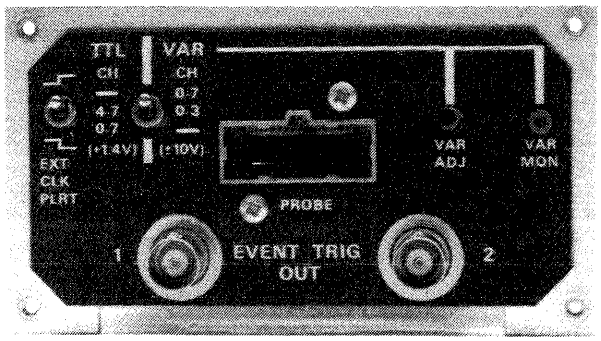
5) Replace the top cover of the 8001/8002 μProcessor Lab. Thread the six screws (previously removed) back into the sides of the cover and tighten.

The Data Acquisition Probe may be connected to the Data Acquisition Interface as needed. The Data Acquisition Probe cable end is keyed to assure proper connection.

DATA ACQUISITION INTERFACE PANEL

The Data Acquisition Interface panel is illustrated in Fig. 8-3. Centrally located on the panel is a 25 pin connector for the Data Acquisition Probe. The P6451 Data Acquisition Probe plug is keyed to insure proper orientation when installed.

Two BNC plugs are located on the lower portion of the panel; and they output Trigger 1 and Trigger 2 pulses.



2393-11

Fig. 8-3. Data Acquisition Interface Panel.

In the upper left hand corner of the panel is a clock polarity switch. This switch selects either the rising or falling edge of the incoming clock signal to latch Probe data within the Interface.

Next to the clock polarity switch is the threshold level switch. When the threshold switch is in the upward position, input channels 0 through 7 are variable from +10 to −10 volts. Adjustment for this variation is made by a potentiometer accessible on the right side of the rear panel. With the threshold switch in the center position channels 0 through 3 are variable and channels 4 through 7 are at a TTL level (+1.4 volts). When the threshold switch is in the lower position, channels 0 through 7 are at a TTL level.

The upper right side of the Data Acquisition Interface panel contains the variable threshold adjustment control and monitor. The monitor jack allows the operator to monitor the variable threshold voltage while adjusting it. Voltage monitoring must be done with a voltmeter having an input impedance of at least 10 M.

JUMPERS/SWITCHES

There are no jumpers or switches on the Real-Time Trace module. An internal jumper located on the Data Acquisition Interface designates clock threshold to be the same as either channel 0 through 3 or channel 4 through 7. See Fig. 8-4 for jumper location.

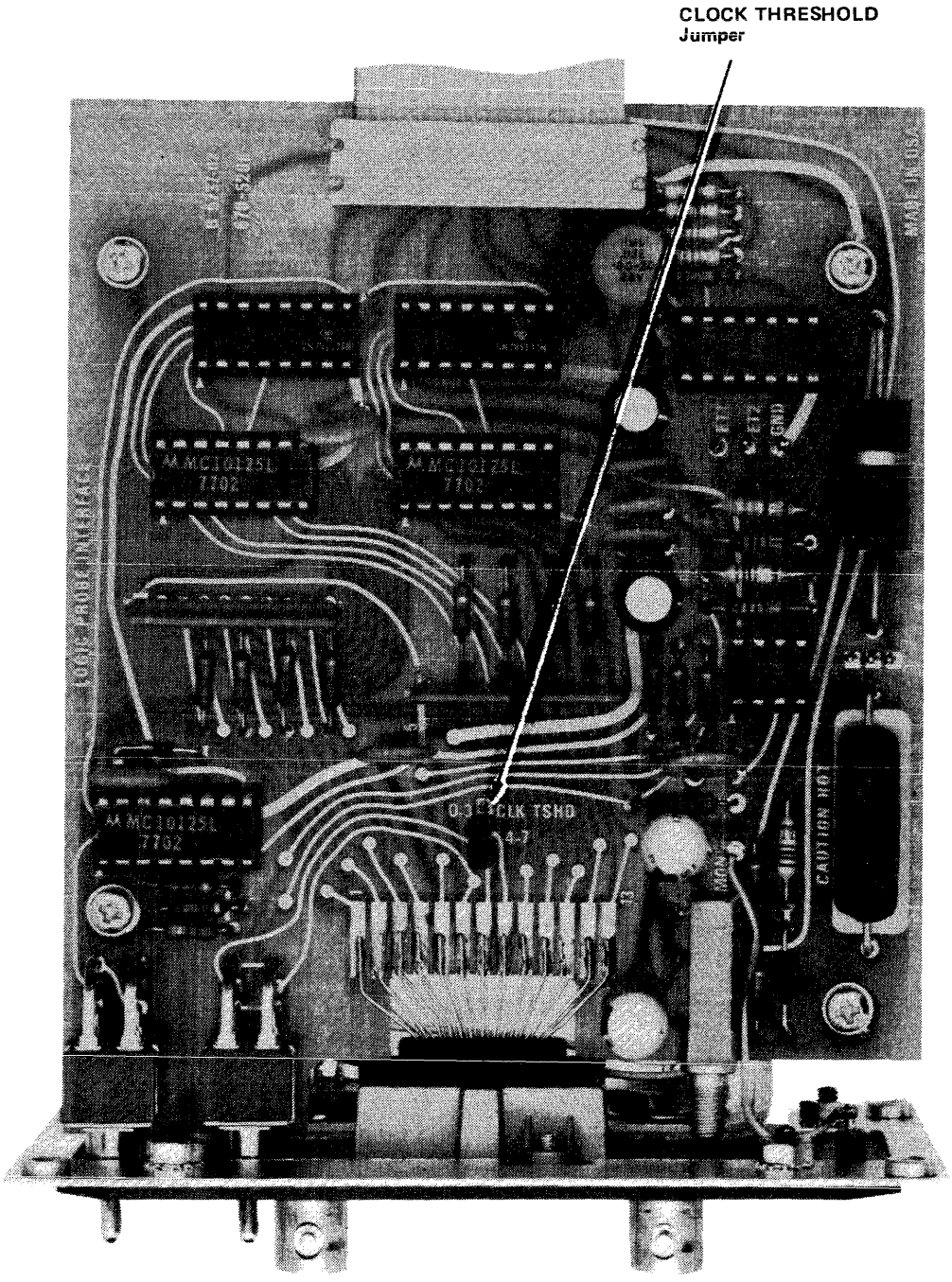


Fig. 8-4. Data Acquisition Interface Board.

Section 9

PROM PROGRAMMER MODULES

INSTALLATION

The PROM Programmer module must be installed in one of two designated slots (J1 or J2) in the 8001 or 8002 μProcessor Lab motherboard. The module edge connector (P1) is offset so that the module won't insert backwards. The physical difference between the PROM Programmer and other modules prevents accidentally plugging other modules into these PROM Programmer slots.

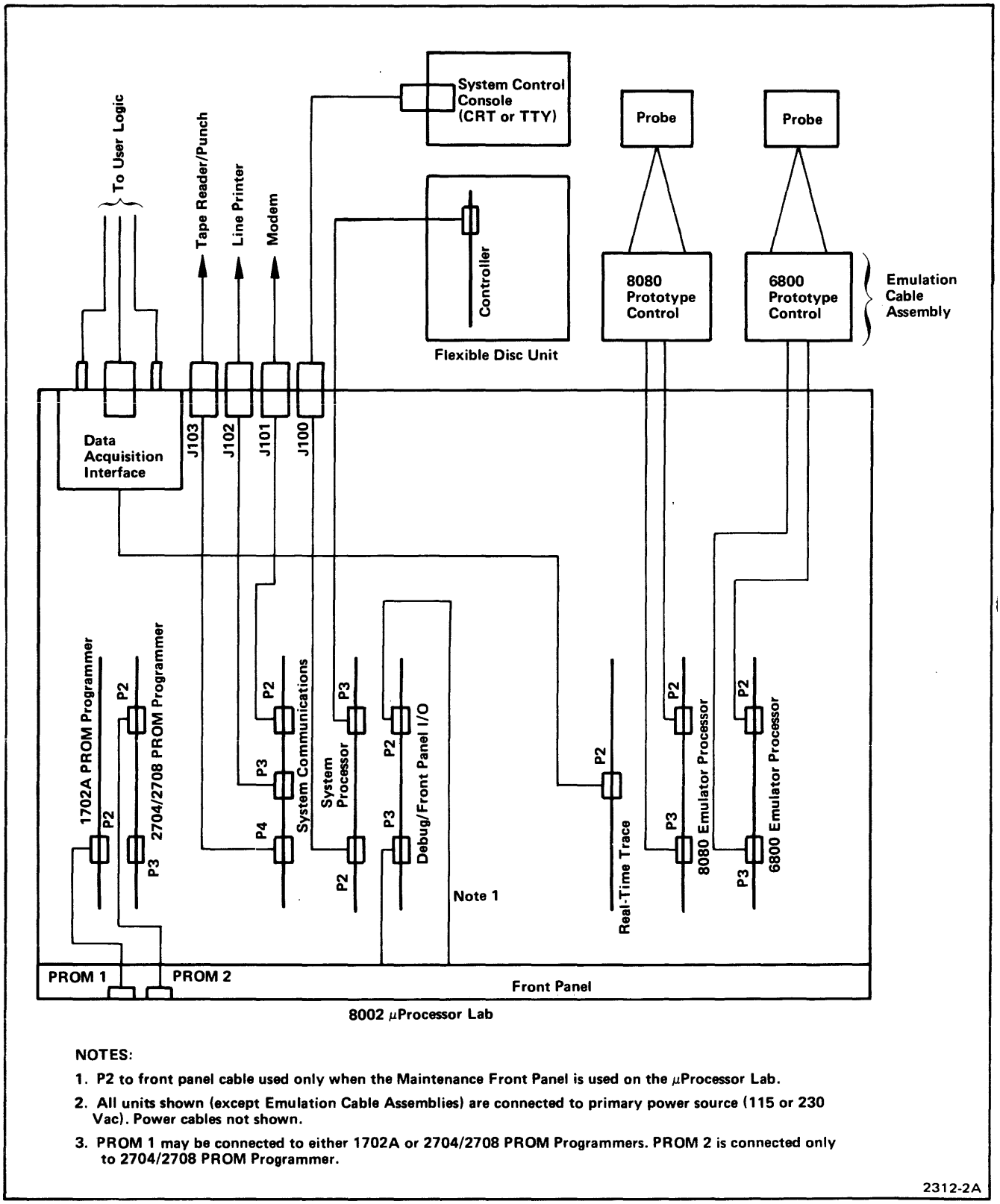
Press down firmly on the plastic lifters until the edge connector snaps into place in the motherboard connector. Plug the cable connector from the front panel PROM sockets as follows:

CAUTION

When attaching the ribbon cable to a PROM Programmer module edge connector, make sure the red strip on the cable and pin 1 of the edge connector are aligned. See Fig. 9-1 for an interconnect diagram.

1702A PROM Programmer

Connect PROM 1 cable connector (26 conductor ribbon cable) to P2 on the 1702A PROM Programmer module.



NOTES:

1. P2 to front panel cable used only when the Maintenance Front Panel is used on the μProcessor Lab.
2. All units shown (except Emulation Cable Assemblies) are connected to primary power source (115 or 230 Vac). Power cables not shown.
3. PROM 1 may be connected to either 1702A or 2704/2708 PROM Programmers. PROM 2 is connected only to 2704/2708 PROM Programmer.

2312-2A

Fig. 9-1. 8001/8002 μProcessor Lab System Interconnect Diagram.

2704/2708 PROM Programmer

Connect PROM 1 cable connector (26 conductor ribbon cable) to P3 and PROM 2 cable connector (40 conductor ribbon cable) to P2 on the 2704/2708 PROM Programmer module.

COMPLEMENTARY ADDRESS AND DATA

In some user prototype instruments, data and address information may be the complement of the data and address information on the buses of the μProcessor Lab. In this situation, the data and/or address from the μProcessor Lab must be complemented before being programmed into the PROM.

1702A Complementary Address And Data

Removing jumper J1 and installing jumper J2 complements the address. To program complementary data into the PROM, jumper J3 must be installed and jumper J4 removed. See Fig. 9-2 for jumper locations. Data information may also be complemented by a software command. See 8001/8002 μProcessor Lab System User's Manual.

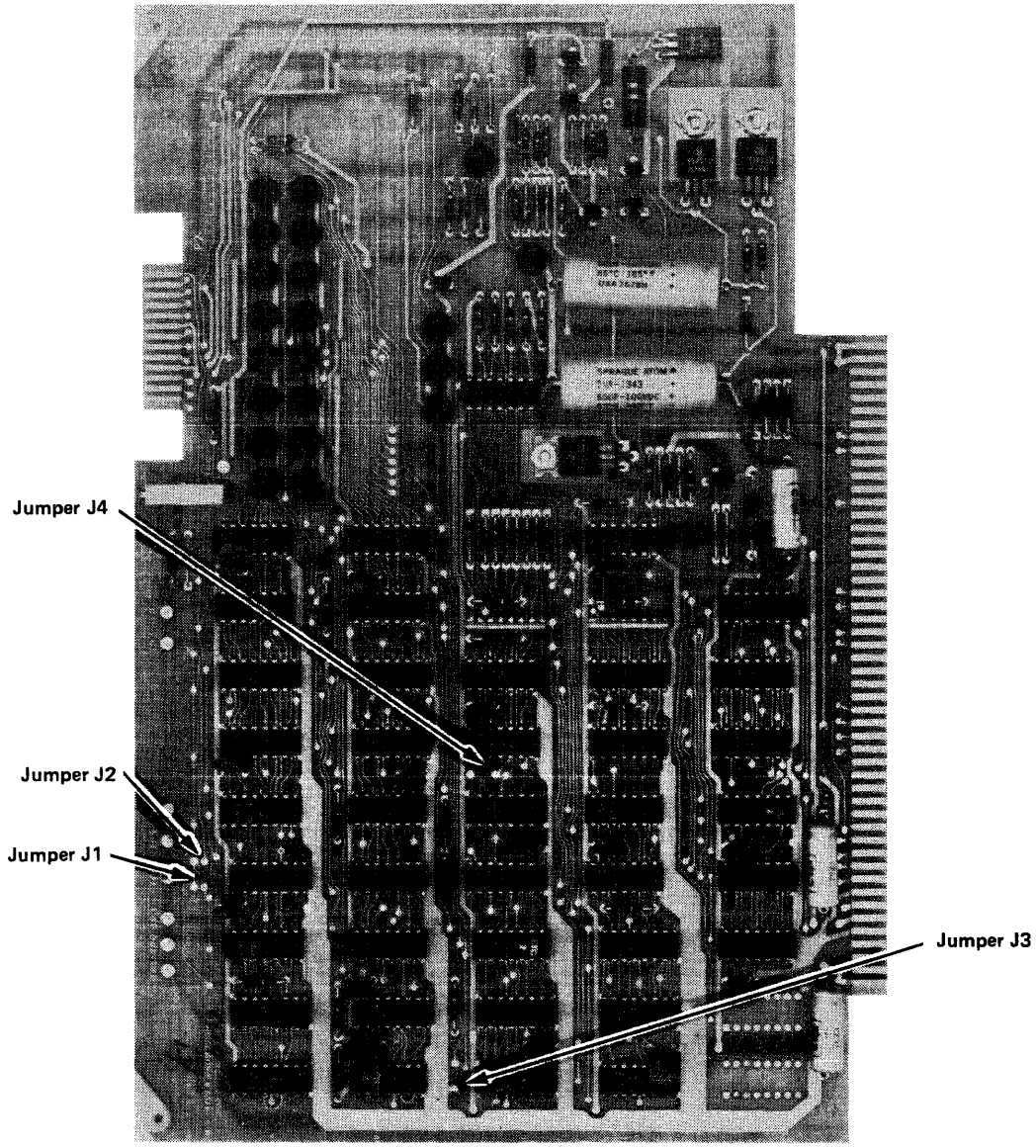
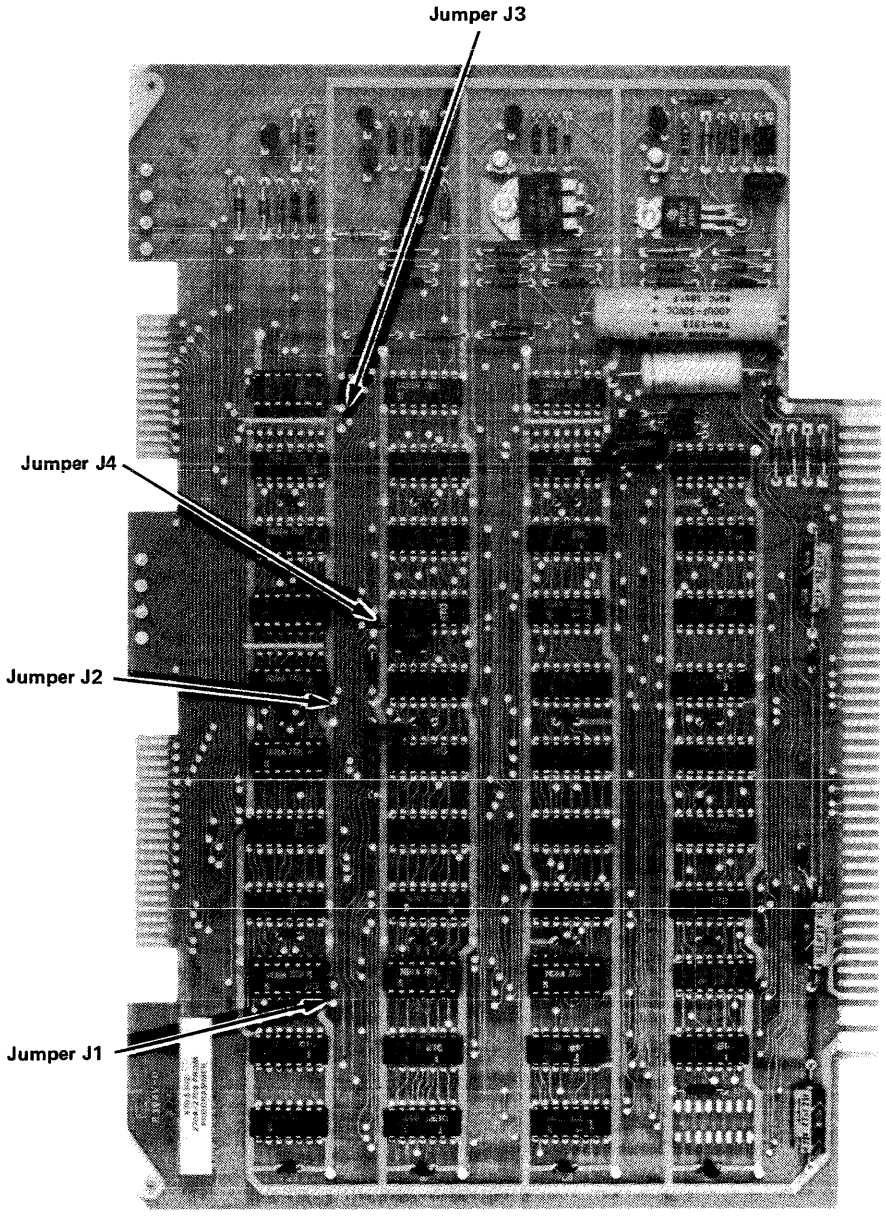


Fig. 9-2. 1702A PROM Programmer Module

2393-13

2704/2708 Complementary Address And Data

Jumper J1 is removed to complement the address. To program complementary data into the PROM, remove jumpers J4, J2 and install jumper J3. See Fig. 9-3 for jumper locations. Data information may also be complemented by a software command. See 8001/8002 μProcessor Lab System User's Manual.



2393-14

Fig. 9-3. 2704/2708 PROM Programmer Module.

Section 10

EMULATOR PROCESSOR MODULES

INSTALLATION

General

The Emulator Processor modules can be installed in any card slot connector in the Program side of the μProcessor Lab motherboard. Emulator Processors are usually installed in slots J17 through J20 (see Fig. 10-1). The card connector is offset to ensure that the module cannot be plugged in backwards. Because of power supply limits, no more than two Emulator Processor modules should be installed in the 60 Hz instruments at one time and only one Emulator Processor should be installed in a 50 Hz (special order) instrument.

CAUTION

Before installing or removing a module, turn the POWER to the μProcessor Lab OFF.

After the module has been correctly positioned, press down firmly on the two plastic lifters (at the board edge) until the 100 pin edge connector (P1) snaps into place and makes a good electrical connection to the motherboard connector.

When using an Emulator Processor, the program memory module must have a module base address of A14 = 0, and A15 = 0. See Program Memory, Section 5, S4163 switch settings.

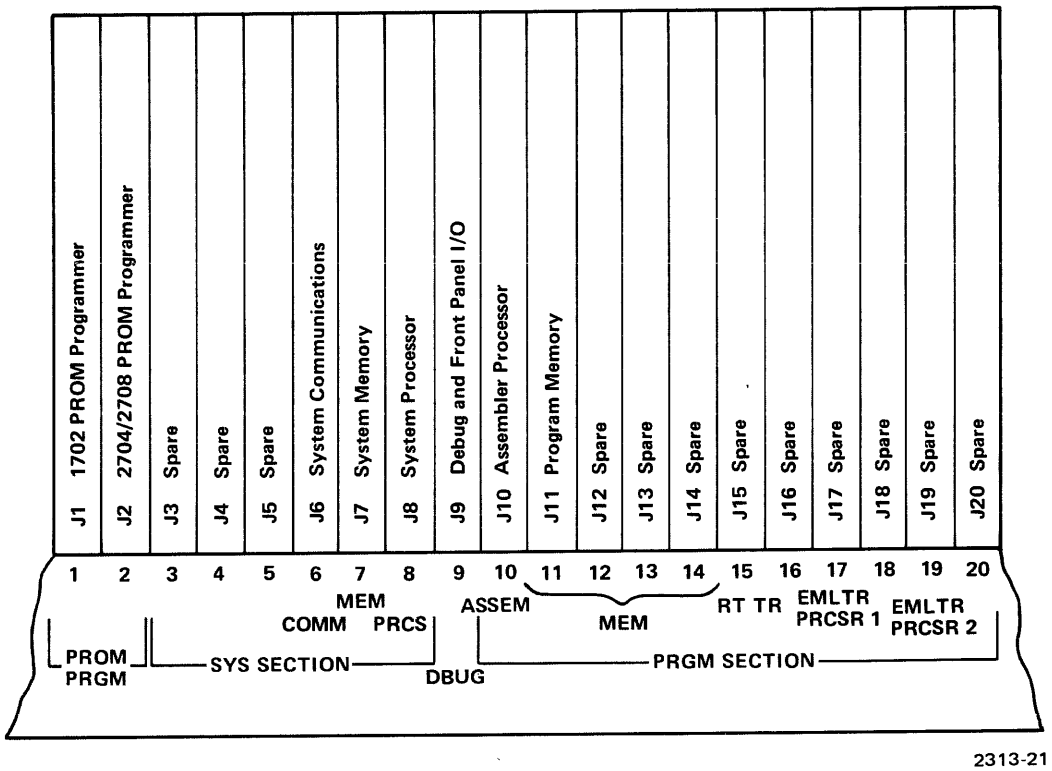


Fig. 10-1. 8001/8002 μProcessor Lab Module Arrangement.

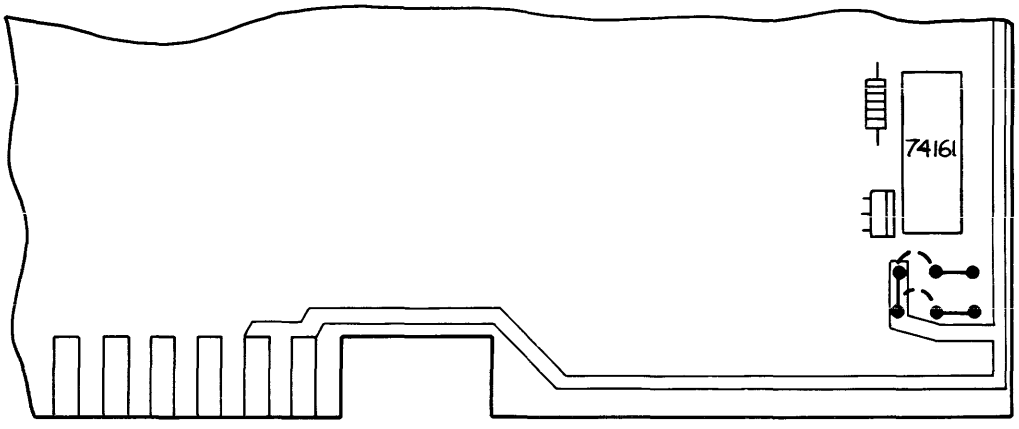
8080 Emulator Processor

No switches or jumper changes. All existing jumpers are configured for the 8001/8002 μProcessor Lab.

6800 Emulator Processor

Jumpers

Two jumper selections may be made on the 6800 Emulator Processor. One selection will control clock rate, the other will disable the on-board RAM. See Fig. 10-2 for jumper locations.



2354-7

Fig. 10-2. 6800 Emulator Processor Clock Rate Jumpers.

Jumpers for a reduced clock rate are provided below position 5180. As supplied, the cycle time is 1 μsec. The upper jumper cut and wired to the left will yield a 1.4 μsec cycle time. Both jumpers wired to the left will yield a 1.6 μsec cycle time.

The jumper between positions (2100 and 2110) can be used to disable the resident RAM function. Cutting this jumper and connecting the pad below (2110) to ground inhibits the RAM. See Fig. 10-3 for jumper location.

Z80 Emulator Processor

Jumpers

Two jumpers are located on the Z80A Emulator Processor module. Both jumpers are present to allow the Z80A Emulator Processor to operate with either the present version of Program Memory, or a new, fast version of Program Memory. See Fig. 10-4.

If the Z80A Emulator Processor is operated at speeds exceeding 2 MHz by the prototype clock (modes 1 and 2), or at 4 MHz with the internal clock (mode 0), and the slow version of Program Memory is being used, J2 must be removed. Removing J2 adds two wait cycles during every Program Memory access. In mode 0 operations, the internal clock may be switched to 2 MHz by removing jumper J1. If the fast version of program memory is used then jumper J1 may be installed to set the internal clock to 4 MHz and jumper J2 should be installed.

9900 Emulator Processor

Jumpers

When the 9900 Emulator Processor module is used with the standard version of the 16k Program Memory, one wait state must be inserted during each memory access. A jumper is provided on the 9900 Emulator Processor module for this function. The faster version of the 16k Program Memory will not require the added wait state except in the debug mode when a wait state is added automatically by software.

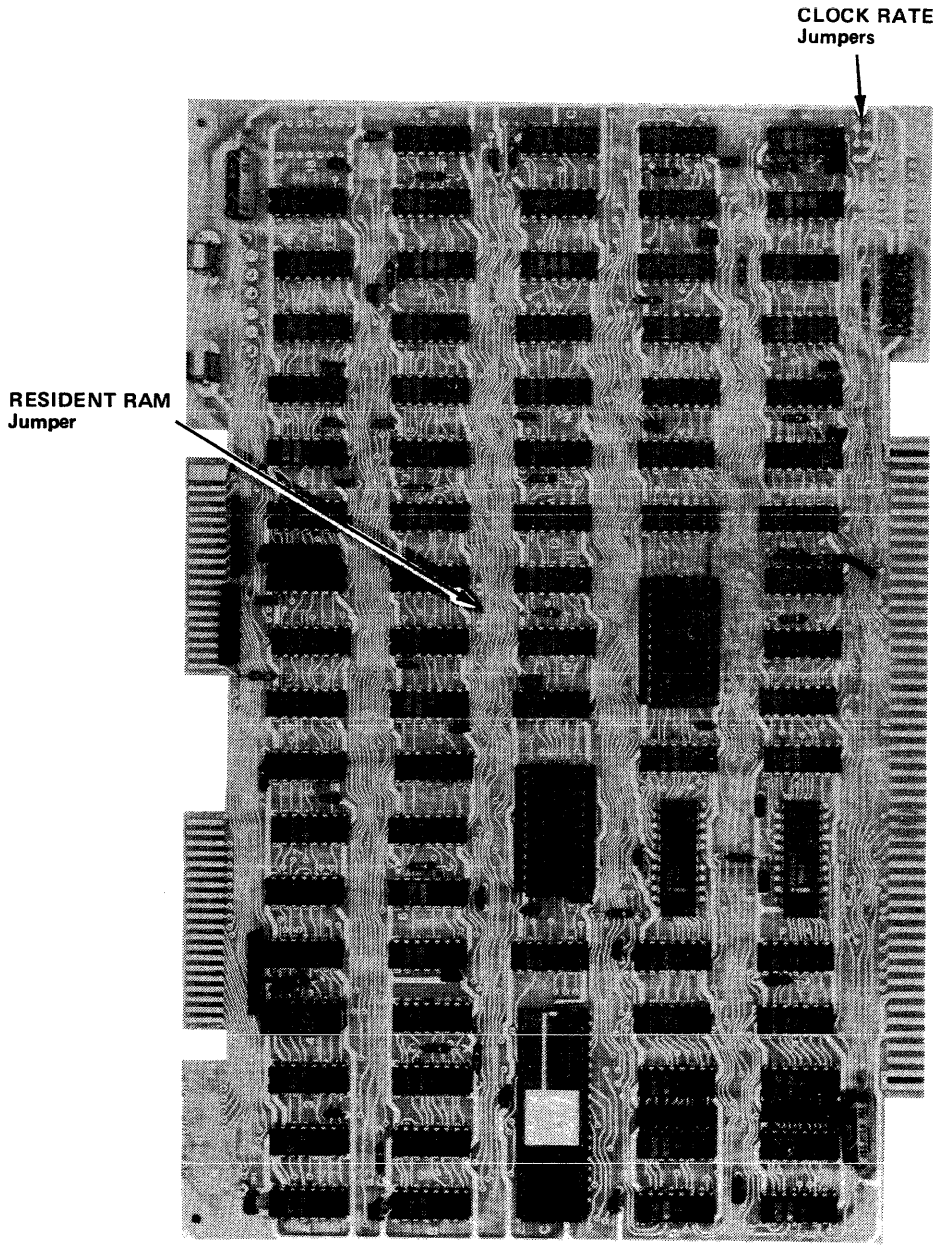


Fig. 10-3. 6800 Emulator Processor Module.

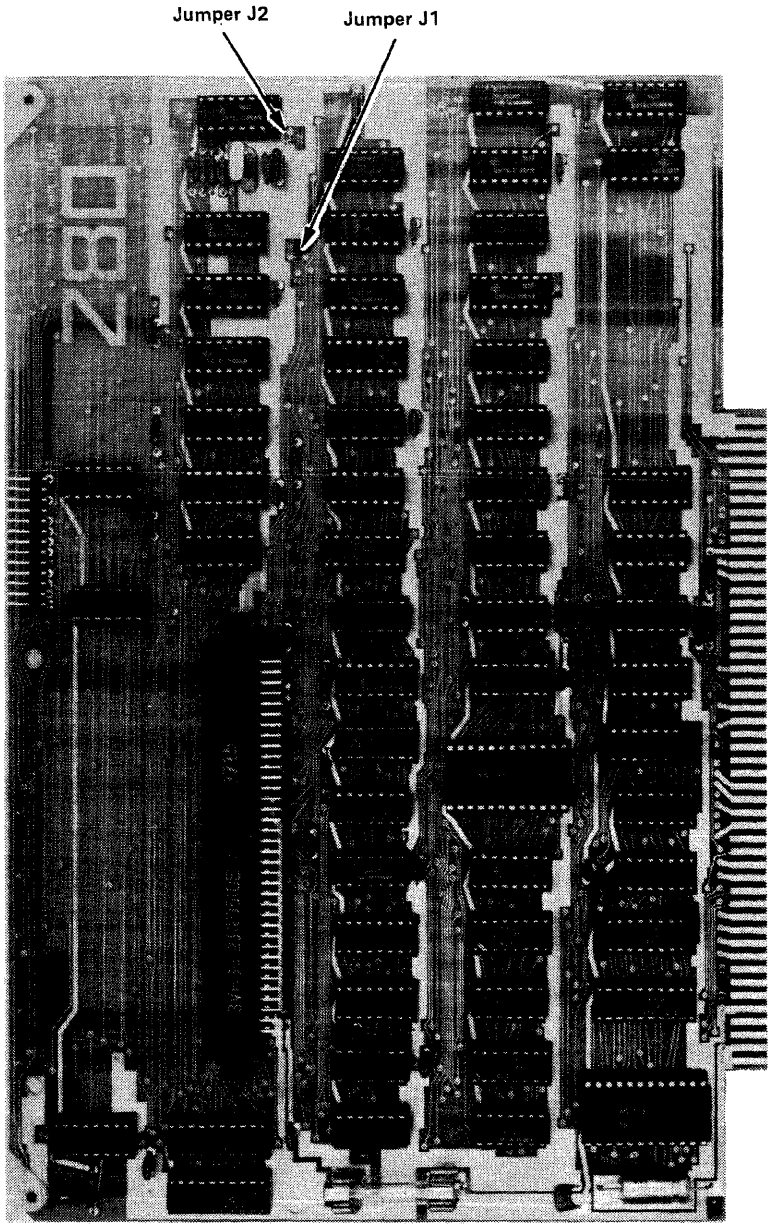


Fig. 10-4. Z80 Emulator Processor Module. 2393-16

One three-function jumper is located on the 9900 Emulator Processor module. This jumper allows the 9900 Emulator Processor to operate with the standard version or new, fast version of Program Memory. In the upper or "Slow" position of the jumper, the 9900 Emulator Processor module will add a wait state* during every memory access except in operating mode 2. Placing the jumper in the lower or "Fast" position allows the 9900 Emulator Processor to run at full speed, adding no wait states except during debug operations. If the jumper is removed entirely, a wait state is added to every memory access regardless of the mode of operation. When the 9900 Emulator Processor is used in conjunction with the Maintenance Front Panel, the jumper must be removed.

*A wait state adds 1/(clock frequency) ns to each memory access.

Section 11

PROTOTYPE CONTROL PROBES

8080, 6800 EMULATOR PROCESSOR

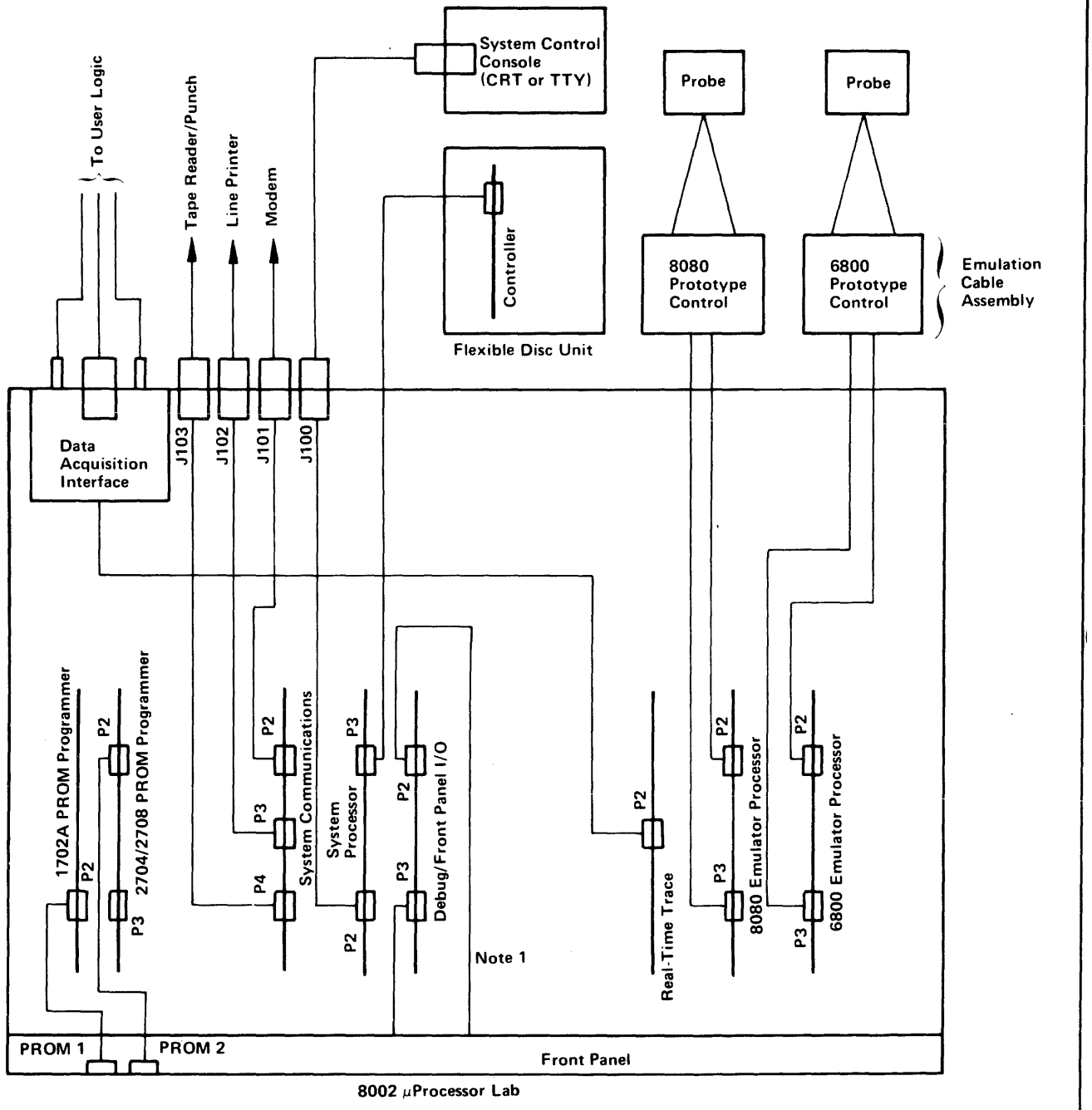
Two Prototype Control Probe cables are attached to the top edge connectors P2 and P3 of the Emulator module as shown in Fig. 11-1. Care should be taken that pin 1 of the cable (red strip) and pin 1 of the edge connector align. Pin 1 is to the left when viewed from the component side of the module. Press firmly on the cable connectors to seat them properly into their board edge connector. Before removing the module, make sure that the primary power to the μProcessor Lab is OFF. Grasp the module ejectors (small white plastic handles on each upper corner of the module) and pull upward. The ejectors will lift the module free of the motherboard.

The emulation cable assemblies that enter the center and right cableways (from a front panel view) on the backpanel of the μProcessor Lab, must be correctly installed in the cable clamps as illustrated in Fig. 11-2. Make sure the bared ground plane of each cable makes good contact with the cable clamps to ensure proper grounding.

9900, Z80 EMULATOR PROCESSOR

The Mobile Microprocessor

An eight-foot cable acts as an interface between the prototype circuitry and the Emulator Processor module. If the microprocessor device remains on the Emulator Processor module, the eight-foot cable could cause an unacceptable time delay. (The Z80A and 9900 operate at excess of 1 MHz.) The potential time delay is eliminated by locating the microprocessor device on a small auxiliary circuit board called the Mobile Microprocessor board.



NOTES:

1. P2 to front panel cable used only when the Maintenance Front Panel is used on the μProcessor Lab.
2. All units shown (except Emulation Cable Assemblies) are connected to primary power source (115 or 230 Vac). Power cables not shown.
3. PROM 1 may be connected to either 1702A or 2704/2708 PROM Programmers. PROM 2 is connected only to 2704/2708 PROM Programmer.

2312-2

Fig. 11-1. 8001/8002 μProcessor Lab System Interconnect Diagram.

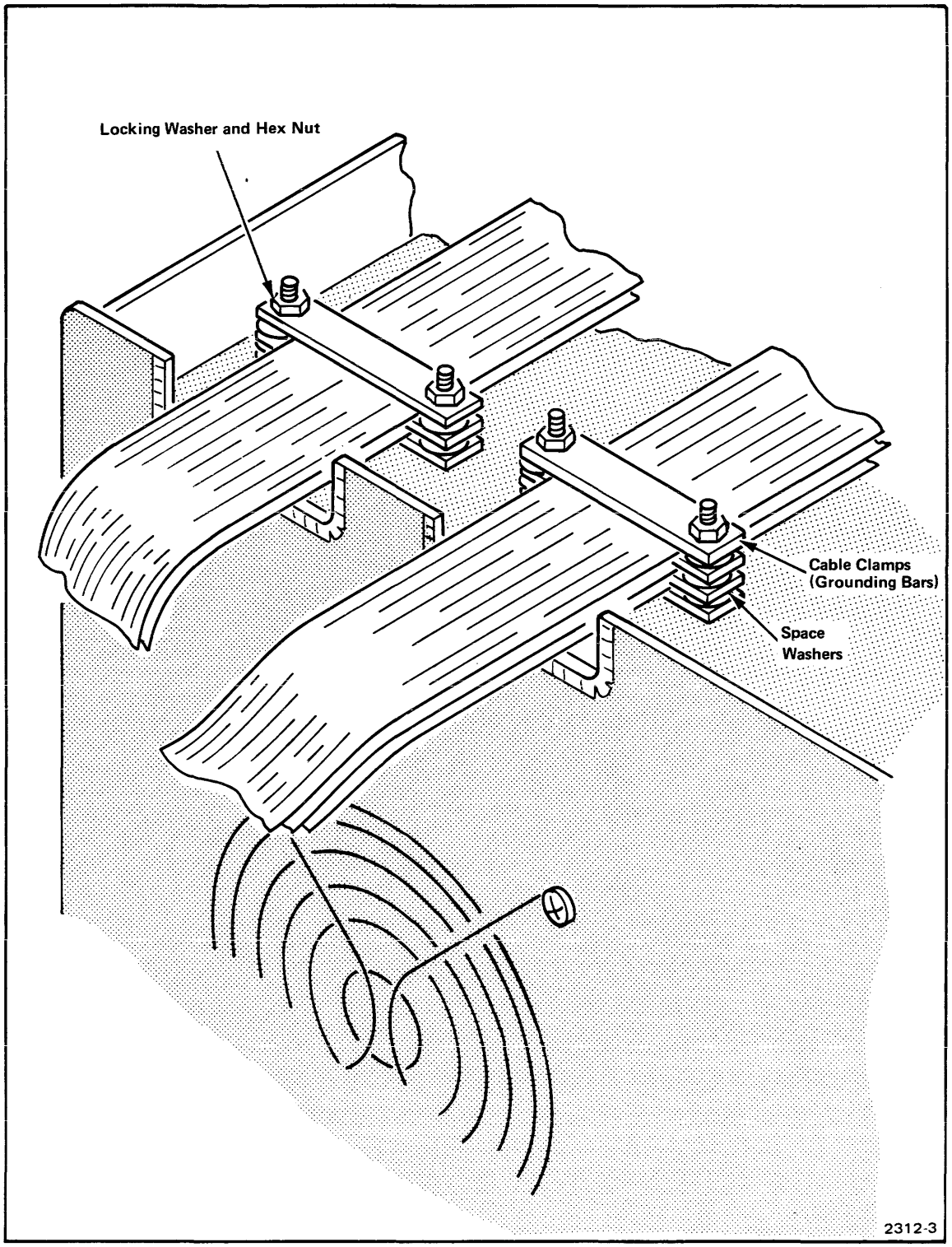


Fig. 11-2. Grounding of Ribbon Interconnect Cables.

When the Emulator Processor module is used in emulation mode 0, the Mobile Microprocessor board is left on the module (see Fig. 11-3). When emulation modes 1 and 2 are used, however, the Mobile Microprocessor board is placed in the interface assembly of the Prototype Control Probe (see Fig. 11-4). With the Mobile Microprocessor board in this position, the distance between the Emulator Processor and the prototype circuit is reduced to 1.5-feet. Delays at 1.5-feet are negligible.

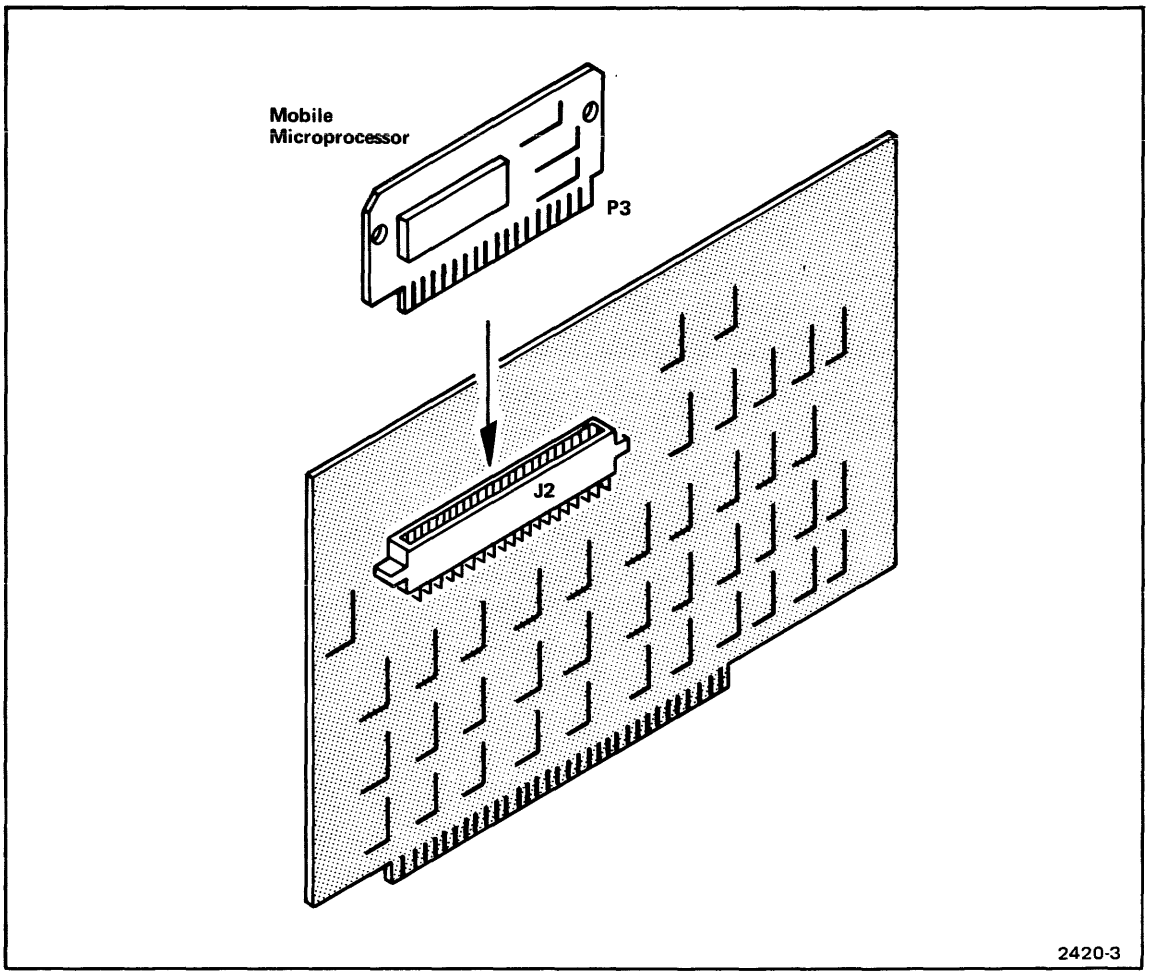


Fig. 11-3. Mobile Microprocessor in Emulation Mode 0.

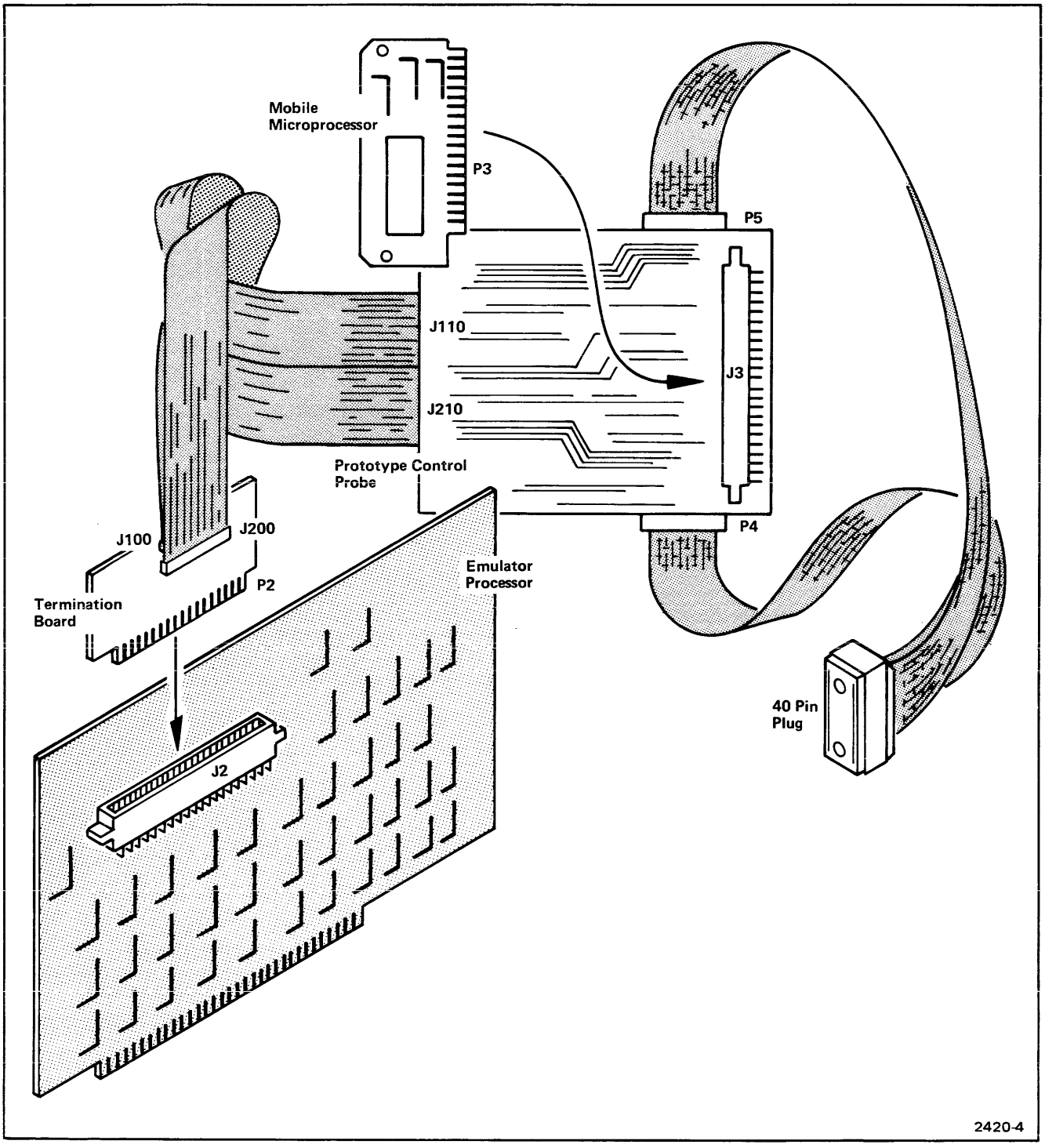


Fig. 11-4. Emulator Processor Emulation Modes 0, 1, and 2.

If a Prototype Control Probe is purchased for use with the Z80 or 9900 Emulator Processor module, the Mobile Microprocessor board is placed permanently within the Prototype Control Probe. The Emulator Processor Module will function in all emulation modes in this configuration.

9900, Z80 Prototype Control Probe

The Z80 or 9900 Emulator Processor Prototype Control Probe consists of:

1) A small termination board.
2) Dual six-foot ribbon cables.
3) The interface assembly: a circuit board containing interface and buffer circuitry and the Mobile Microprocessor board.
4) Two 1.5-foot ribbon cables.
5) A 40-pin plug.

Fig. 11-5 illustrates the Prototype Control Probe.

The termination board plugs into the socket on the Z80 or 9900 Emulator Processor module vacated by the Mobile Microprocessor board. Two six-foot ribbon cables are attached to the termination board. The ribbon cables connect to the circuit board located inside the Probe interface assembly.

The 40-pin plug is designed to fit into the prototype circuit Z80 socket. The plug has a spring plate on the bottom that slides over the pins for protection against damage. When the plug is inserted into a socket, the protective plate retracts into the body of the plug.

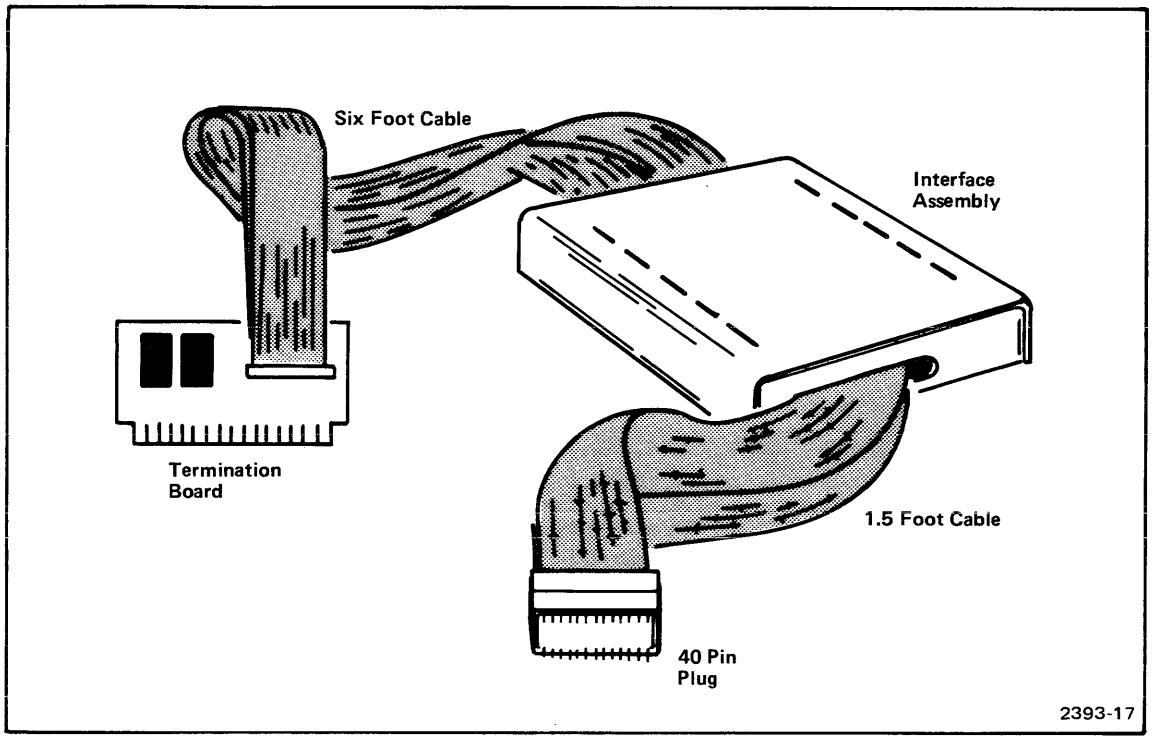


Fig. 11-5. 9900/Z80 Prototype Control Probe.

INSTALLATION

If a Prototype Control Probe is to be installed with the Emulator Processor module the Mobile Microprocessor board must be placed in the interface assembly of the Prototype Control Probe before installing the Emulator Processor module.

The Prototype Control Probe is installed in the following manner:

1) Lay the Emulator Processor module on a flat surface, component side up.

2) Notice the Mobile Microprocessor board plugged into connector J2. Remove the two (2) screws mounting the Mobile Microprocessor board to the Emulator Processor module.

3) Remove the Mobile Microprocessor board from socket J2. This is accomplished by inserting a small flat-bladed screwdriver between the Mobile Microprocessor board and the corner of socket J2. Pry up gently until the Mobile Microprocessor board comes free of the socket.

4) Lay the Mobile Microprocessor board aside on a conductive material such as pink polyethylene.

CAUTION

The microprocessor device located on the Mobile Microprocessor board is subject to damage by static discharge when the board is not in a socket. Care should be taken when handling the Mobile Microprocessor board. Hold the circuit board by its edges only. When storing or shipping the Mobile Microprocessor board, wrap the board in a conductive material such as conductive foam or pink polyethylene.

5) A small termination board is located at the end of the long Prototype Control Probe cable. Insert the termination board into socket J2, ensuring pin 1 of the termination board edge connector is aligned with pin 1 of socket J2.

6) Insert the two screws (removed in step 3) through the mounting holes of the termination board. Thread the screws into the Emulator Processor module and tighten gently.

7) Mount the Emulator Processor module in the μProcessor Lab. The emulation cable assemblies that enter the center and right cableways (from a front panel view) on the backpanel of the μProcessor Lab, must be correctly installed in the cable clamps as illustrated in Fig. 11-1. Make sure the bared ground plane of each cable makes good contact with the cable clamps to ensure proper grounding.

The Mobile Microprocessor board is mounted in the Prototype Control Probe interface assembly in the following manner:

1) Unscrew the four (4) rubber feet on the bottom of the interface assembly.

2) Lift the cover of the interface assembly and set it aside.

3) Unplug connectors J4 and J5.

4) Notice six (6) screws, three down each side of the interface assembly circuit board. Remove the six screws.

5) Lift the circuit board up and notice socket J3 on the back side of the board.

6) Insert the Mobile Microprocessor board edge connector into socket J3. Make sure the component side of the Mobile Microprocessor board is facing out.

7) Using the two (2) mounting screws from the Emulator Processor module, fasten the Mobile Microprocessor board to the interface assembly circuit board.

8) Re-assemble the interface assembly in the reverse order of the steps just listed.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime	108 - 10 V output pulse 1 ns Risetime
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay
PG 508 replaces 114	Performance of replacement equipment is the same or better than equipment being replaced.	
115		
2101		
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191		
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
SG 504 replaces 067-0532-01	SG 504 - Frequency range 245 MHz to 1050 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
067-0650-00		
TG 501 replaces 180, 180A	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181		181 - Multiple time-marks
184	TG 501 - Trigger output-slaved to market output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Separate trigger pulses of 1 and 0.1 sec; 10, 1, and 0.1 ms; 10 and 1 μs.
2901	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

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MANUAL CHANGE INFORMATION

PRODUCT 8001/8002 µProcessor Lab Installation Guide

CHANGE REFERENCE C1/1177

DATE 11-21-77

CHANGE: DESCRIPTION

070-2393-02 & 070-2717-00

TEXT CORRECTION

Please insert the following table on page 5-3 immediately following Table 5-1 and on page 6-3 immediately following Table 6-1. When inserting on page 6-3, change the table head to read TABLE 6-1A.

TABLE 5-1A

MEMORY MODULE OPTION SWITCH FUNCTIONS

S4163-1	S4163-2	Memory Module
S4140-2	S4140-1	Starting address
OFF	OFF	ØØØØ
ON	OFF	4ØØØ
OFF	ON	8ØØØ
ON	ON	CØØØ

Note: Switch S4163 settings apply to the Program Memory 1 8002 System Memory Module. Switch S4140 settings apply to the High Speed Memory module.

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MANUAL CHANGE INFORMATION

Change Reference: C2/279 Date: 2-20-79

Product: 8001/8002A µP LAB INSTALL GUIDE 070-2717-00

CHANGE	DESCRIPTION

ADD the following note to these two pages:

1. Page 5-1, after the Installation information.
2. Page 6-1, after the Installation information.

NOTE

Reliability is reduced if 8002A µProcessor Lab Program Memory modules are reconfigured for System Memory operation, or vice-versa.

Reliability will also be reduced with the 8001 or 8002A if Program Memory is made up of both High-Speed and 16K Dynamic RAM modules.